

Figuras do Capítulo 13

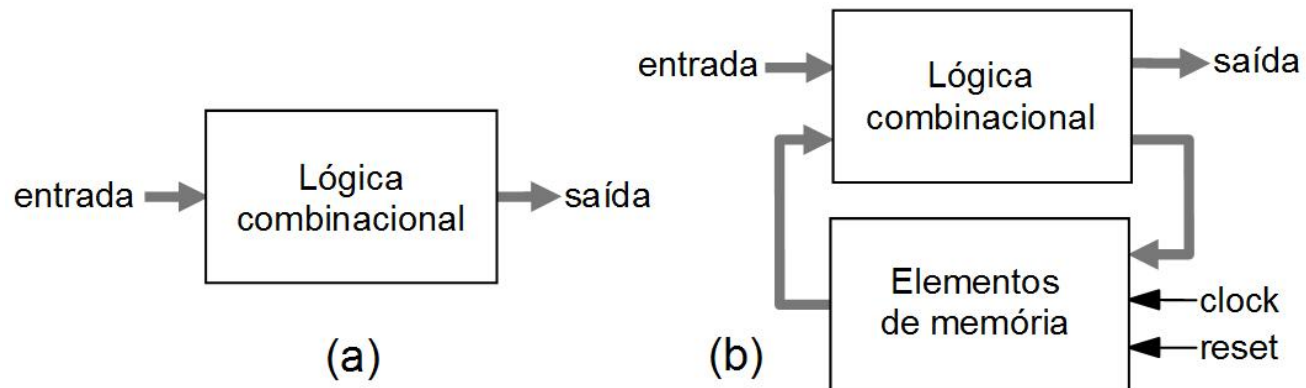


Figura 13.1

Figuras do Capítulo 13

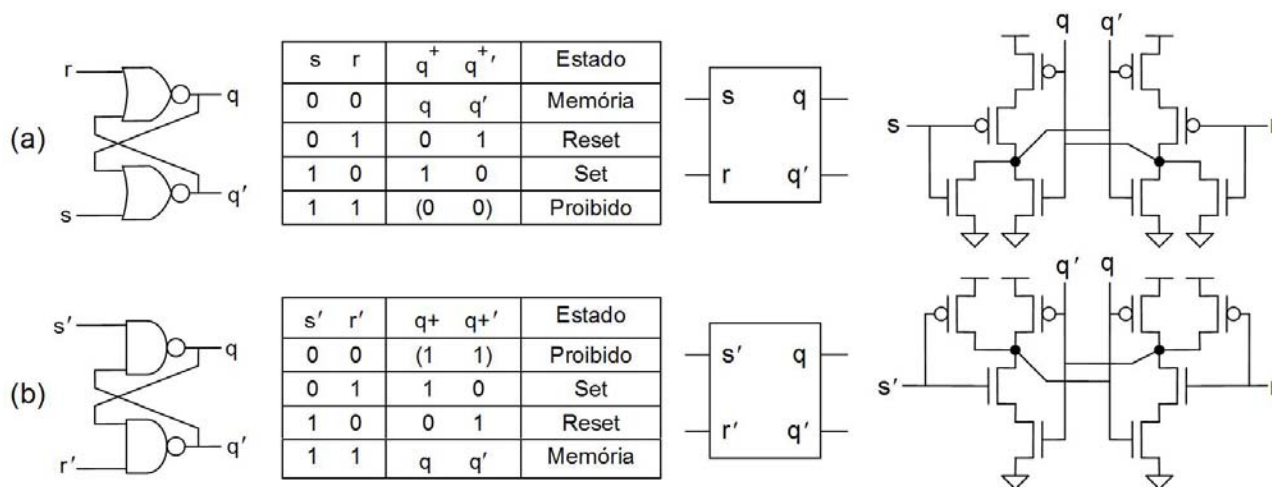


Figura 13.2

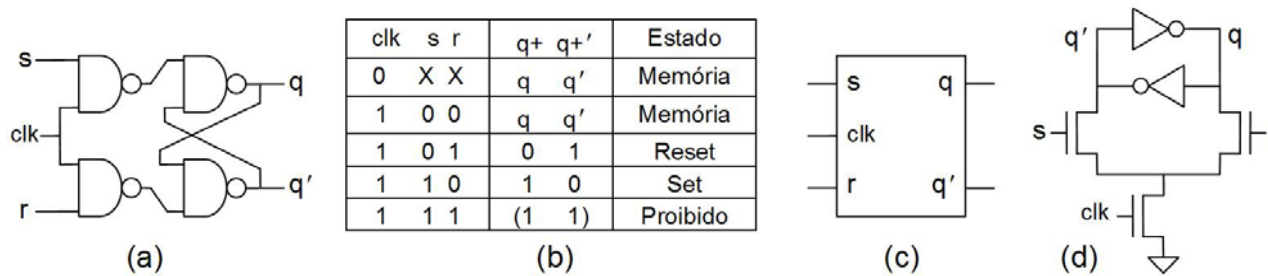


Figura 13.3

Figuras do Capítulo 13

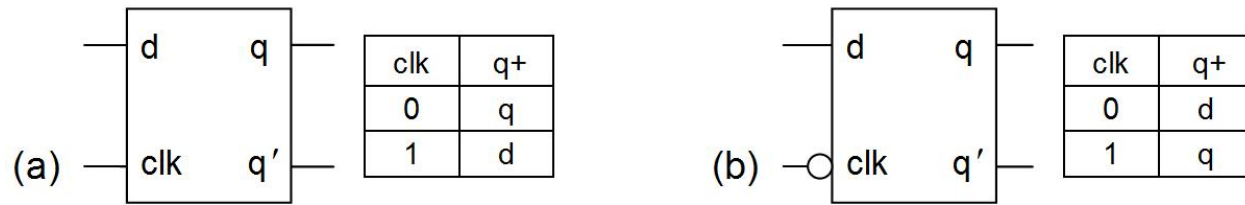


Figura 13.4

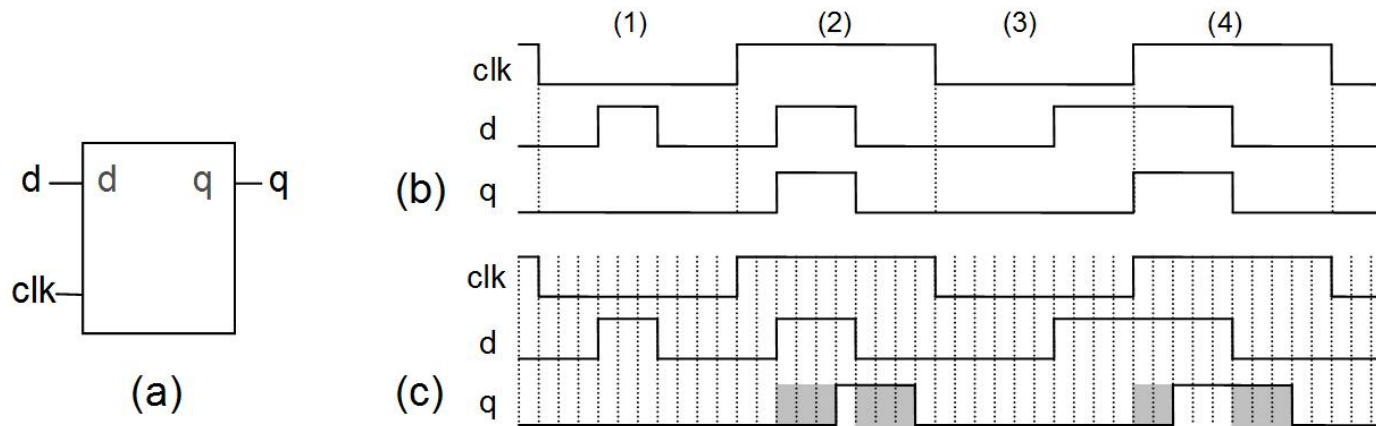


Figura 13.5

Figuras do Capítulo 13

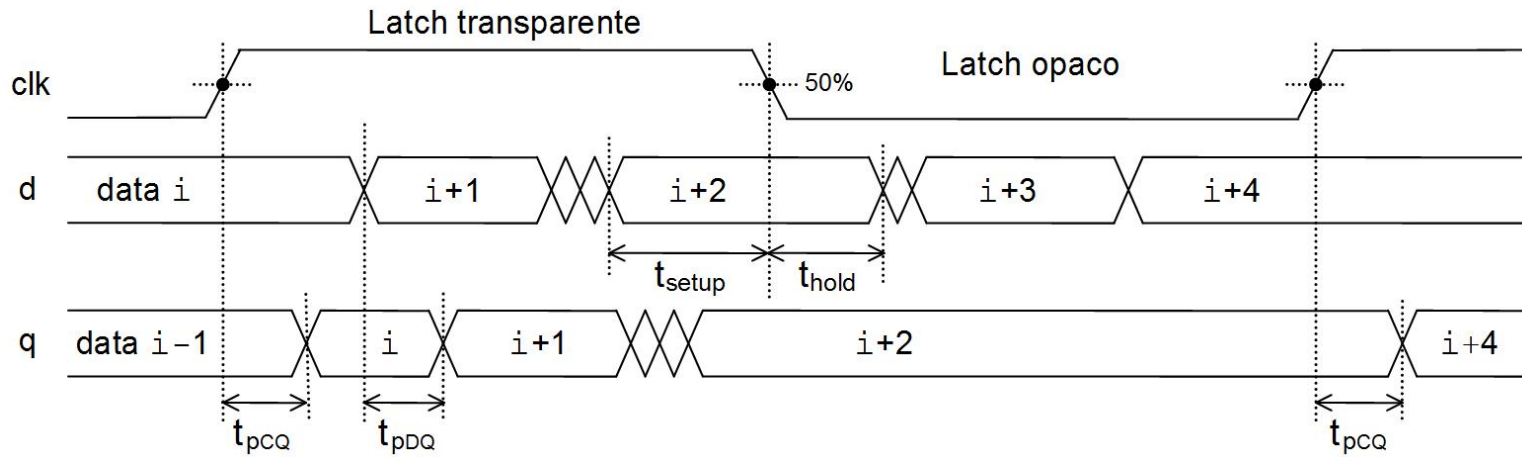


Figura 13.6

Figuras do Capítulo 13

Grupo		Nome do latch		Figura	Bibliografia
DLs estáticos	Baseado em mux	Explicit mux-based latch		13.8(a)	
		STG	Static TG-based latch	13.8(b)	[Rabaey03]
		TG-C ² MOS	TG-C ² MOS-based latch	13.8(c)	[Weste05]
		NAND latch	NAND-based latch	13.8(d)	
	Tipo RAM	SRAM	SRAM-based latch	13.8(e)	(Sec. 4.2)
		S-STG	Simplified STG latch	13.8(f)	[Weste05]
		Jamb	Jamb latch	13.8(g)	[Dike99, Kinniment02]
		S-CVSL	Static Cascode Volt. Switch Logic latch	13.8(h)	
		SRIS	Static Ratio Insensitive latch	13.8(i)	[Yuan97]
		SSTC1	Static Single Transistor Clocked 1 latch	13.8(j)	[Yuan97]
		SSTC2	Static Single Transistor Clocked 2 latch	13.8(k)	[Yuan97]
	Modo corrente	ECL	Emitter Coupled Logic latch	13.8(l)	[Mizuno92, Knapp01]
SCL		Source Coupled Logic latch	13.8(m)	[Mizuno92, Knapp01]	
DLs dinâmicos	DTG1	Dynamic TG-based 1 latch	13.9(a)	[Weste05]	
	DTG2	Dynamic TG-based 2 latch	13.9(b)	[Weste05]	
	C ² MOS	C ² MOS-based latch	13.9(c)	[Weste05]	
	TSPC	True Single Phase Clock latch	13.9(d)	[Yuan89]	
	CVSL	Cascode Voltage Switch Logic latch	13.9(e)	[Weste05]	
	DSTC1	Dyn. Single Transistor Clocked 1 latch	13.9(f)	[Yuan89]	
	DSTC2	Dyn. Single Transistor Clocked 2 latch	13.9(g)	[Yuan89]	

Figura 13.7

Figuras do Capítulo 13

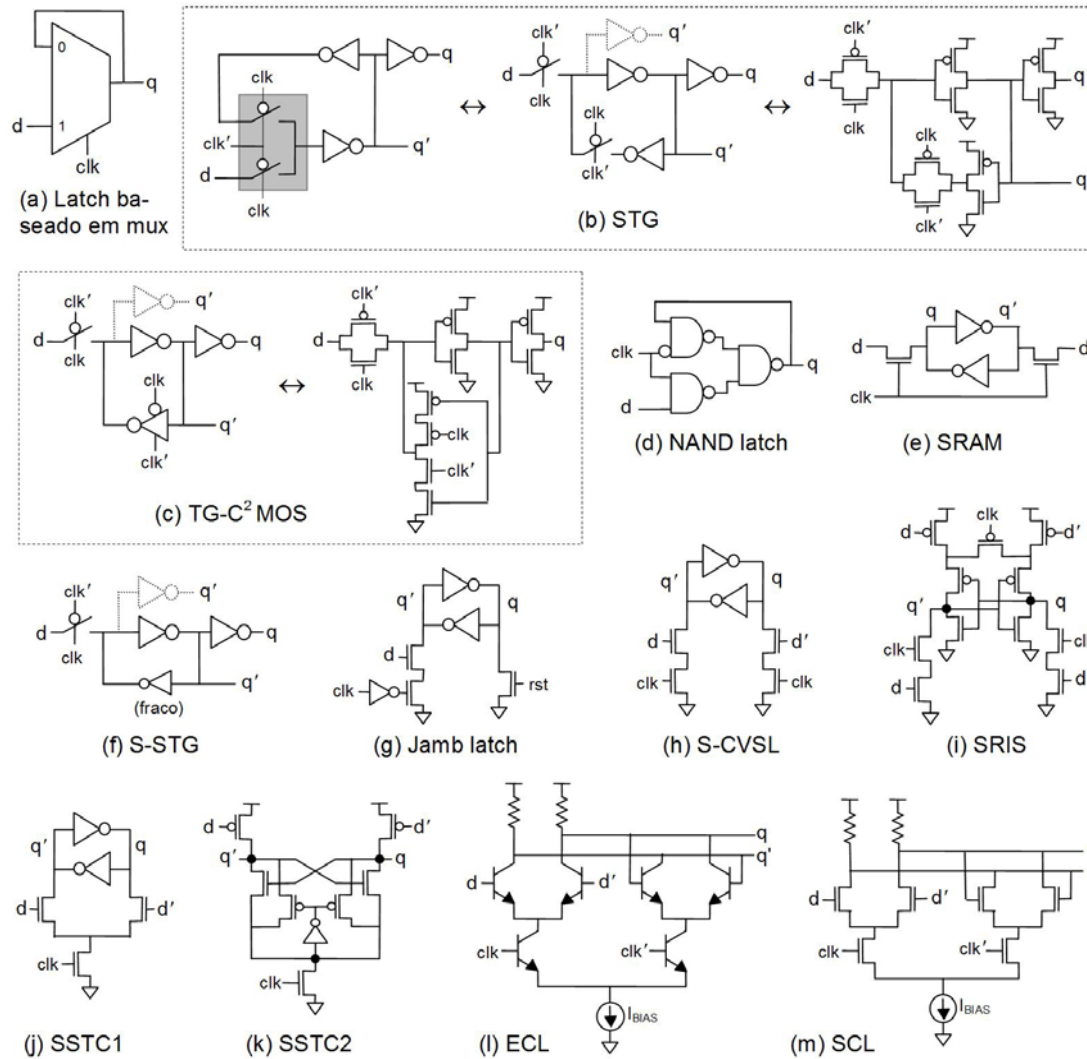


Figura 13.8

Figuras do Capítulo 13

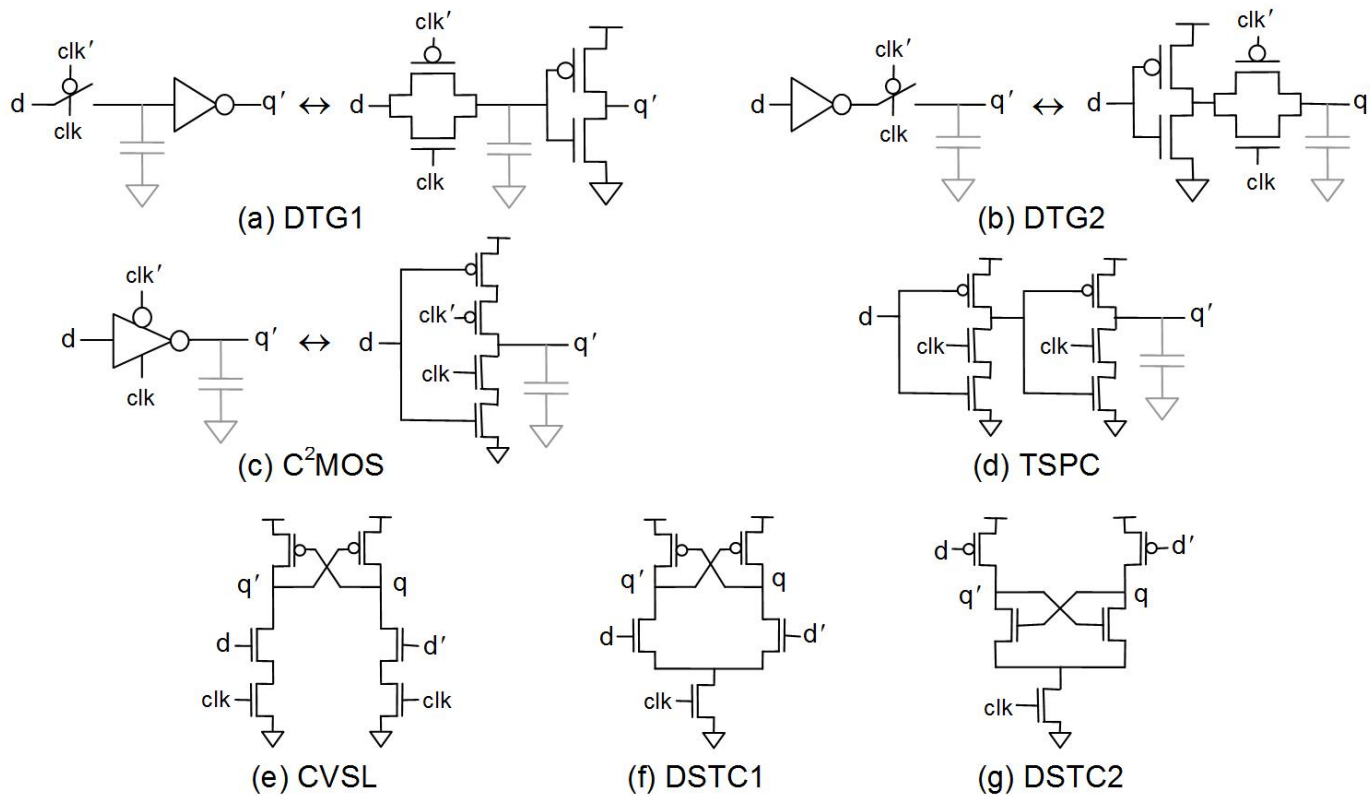


Figura 13.9

Figuras do Capítulo 13

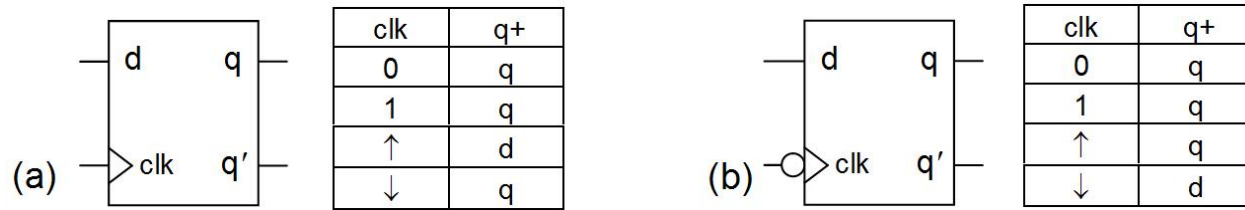


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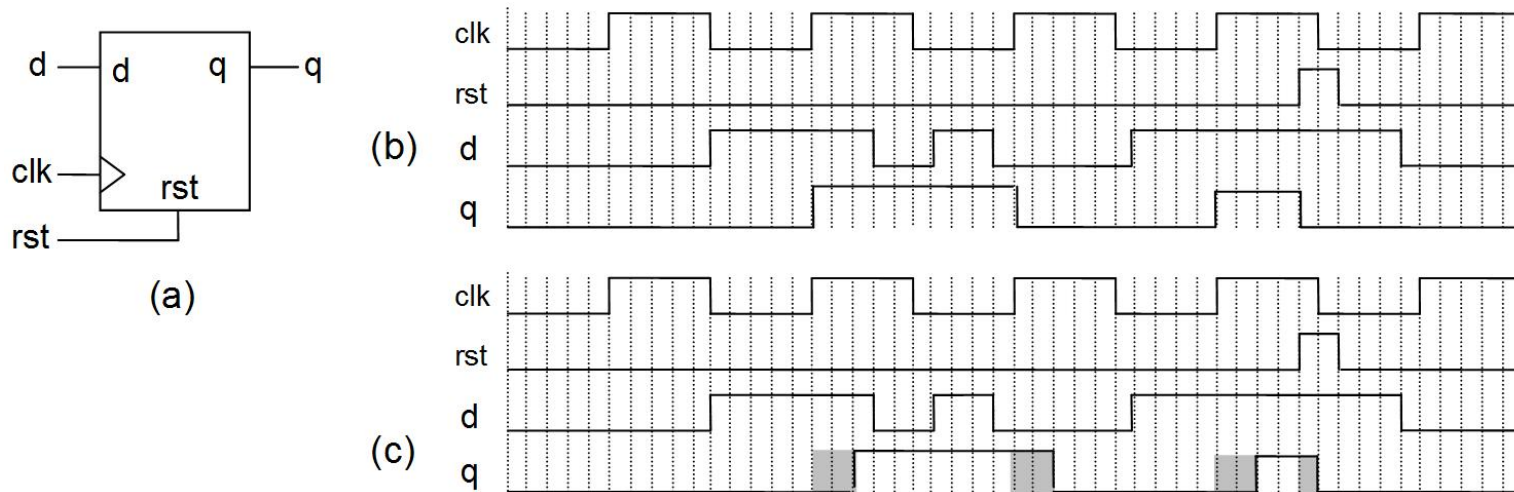


Figura 13.11

Figuras do Capítulo 13

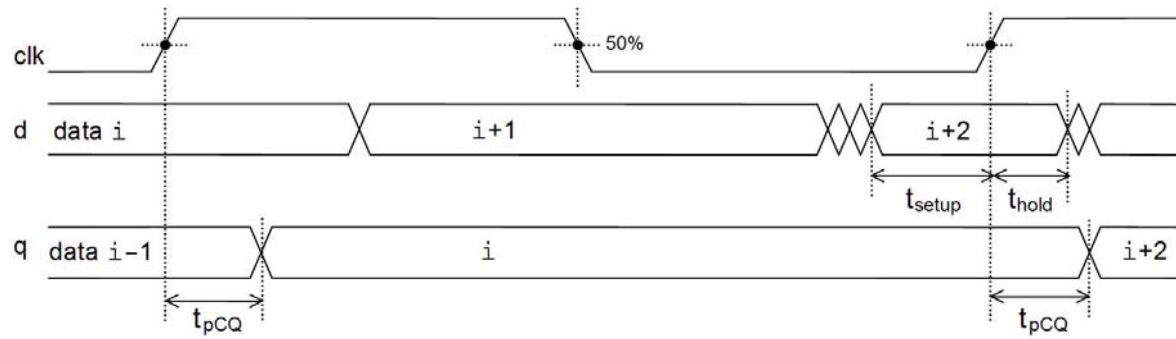


Figura 13.12

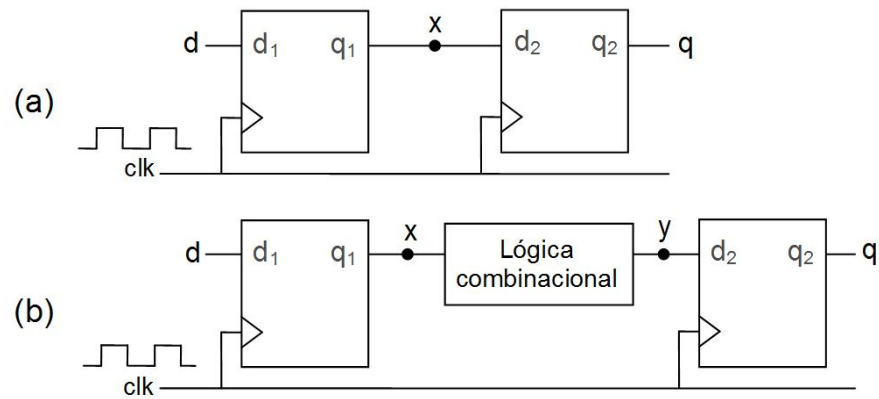


Figura 13.13

Figuras do Capítulo 13

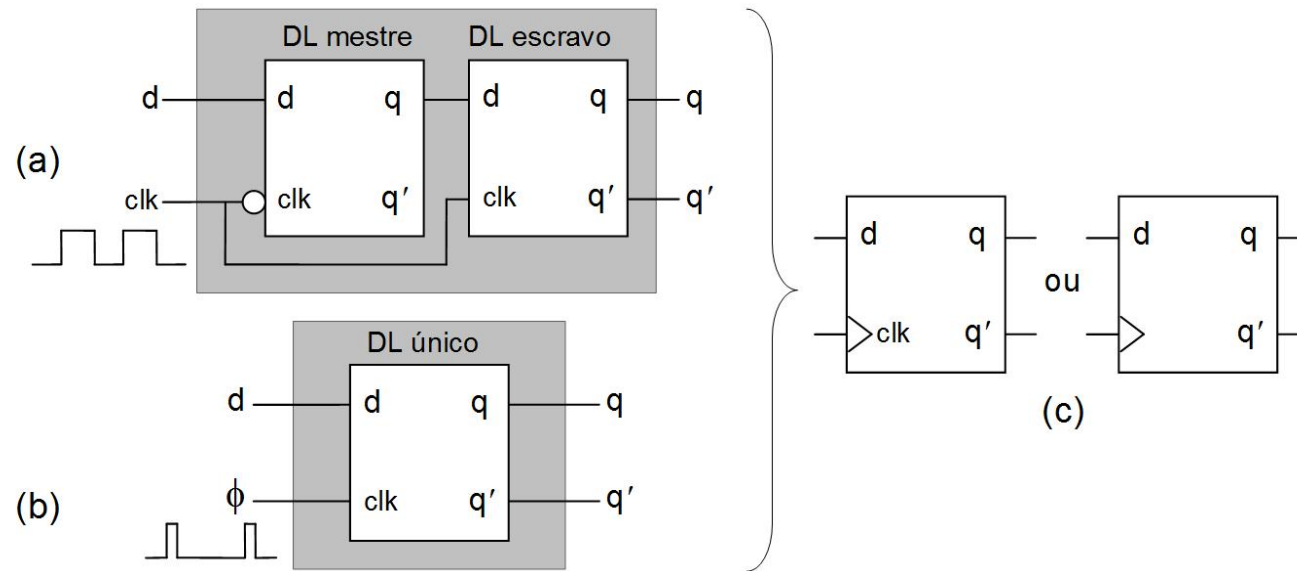


Figura 13.14

Figuras do Capítulo 13

Grupo	Nome do flip-flop		Figura	Bibliografia
Tipo mestre-escravo convencionais	DTG	Dynamic Transmission-Gate-based flip-flop	13.16(a)	[Rabaey03]
	C ² MOS	C ² MOS-based flip-flop	13.16(b)	[Rabaey03, Weste05]
	STG	Static Transmission-Gate-based flip-flop	13.16(c)	[Rabaey03, Weste05]
	TG-C ² MOS	TG/C ² MOS-based flip-flop (PowerPC 603 proc.)	13.16(d)	[Gerosa94]
Tipo mestre-escravo especiais	TSPC	True Single Phase Clock flip-flop	13.17(a)	[Yuan89]
	E-TSPC	Enhanced TSPC flip-flop	13.17(b)	[Huang96]
	GF-TSCP	Glitch-Free TSPC flip-flop	13.17(c)	[Huang96]
	DSTC	Dynamic Single Transistor Clocked flip-flop	13.17(d)	[Yuan97]
	SSTC	Static Single Transistor Clocked flip-flop	13.17(e)	[Yuan97]
	SAFF	Sense-Amplifier-based Flip-Flop	13.17(f)	[Matsui94]
	StrongARM	Flip-flop used in the StrongARM 110 processor	13.17(f)	[Montanaro96]
	Nikolic SAFF	Modified Nikolic SAFF flip-flop	13.17(f)	[Nikolic00]
	Kim SAFF	Modified Kim SAFF flip-flop	13.17(f)	[Kim00]
	Strollo SAFF	Modified Strollo SAFF flip-flop	13.17(f)	[Strollo05]
	ECL	Emitter-Coupled-Logic-based flip-flop	13.17(g)	[Knapp01, Wang06]
	SCL	Source-Coupled-Logic-based flip-flop	13.17(h)	[Heydari06, Kromer06]
	S-SCL	Simplified SCL flip-flop	13.17(h)	[Shu02, Peng07]
Baseados em pulsos	EP/TG-C ² MOS	Expl.-Pulsed TG-C ² MOS-based flip-flop (NEC RISC proc.)	13.19(a)	[Kozu96]
	HLFF / Partovi	Hybrid Latch Flip-Flop or Partovi flip-flop (K6 proc.)	13.19(b)	[Partovi96]
	K6	Self-resetting flip-flop also used in the AMD K6 proc.	13.19(c)	[Draper97]
	SDFF / Klass	Semi-Dynamic Flip-Flop or Klass flip-flop	13.19(d)	[Klass99]
	DSETL	Dual-rail Static Edge-Triggered Latch	13.19(e)	[Ding01]
	Itanium 2 / Montecito	Flip-flop used in the Itanium 2 and Itanium Montecito proc.	13.19(f)	[Naffziger02, 05]
Flip-flops de borda dupla	Mux-based	Mux-based dual-edge flip-flop	13.20(a)	
	DE/TG-C ² MOS	Dual-Edge TG-C ² MOS-based flip-flop	13.20(b)	
	IP-SRAM	Implicit-Pulsed SRAM-based dual-edge flip-flop	13.20(c)	[Moisiadis01]
	DSPFF	Dual-edge-triggered Static Pulsed Flip-Flop	13.20(d)	[Ghadiri05]
	DESPFF	Dual-Edge-triggered Static Pulsed Flip-Flop	13.20(e)	[Ghadiri05]
Com consumo estatisticamente reduzido	GCFF	Gated-Clock Flip-Flop	13.21(a)	[Strollo00]
	CCFF	Conditional-Capture Flip-Flop	13.21(b)	[Kong01]
	DCCER	Dif. Conditional-Capture Energy-Recovery flip-flop	13.21(c)	[Cooke03]

Figura 13.15

Figuras do Capítulo 13

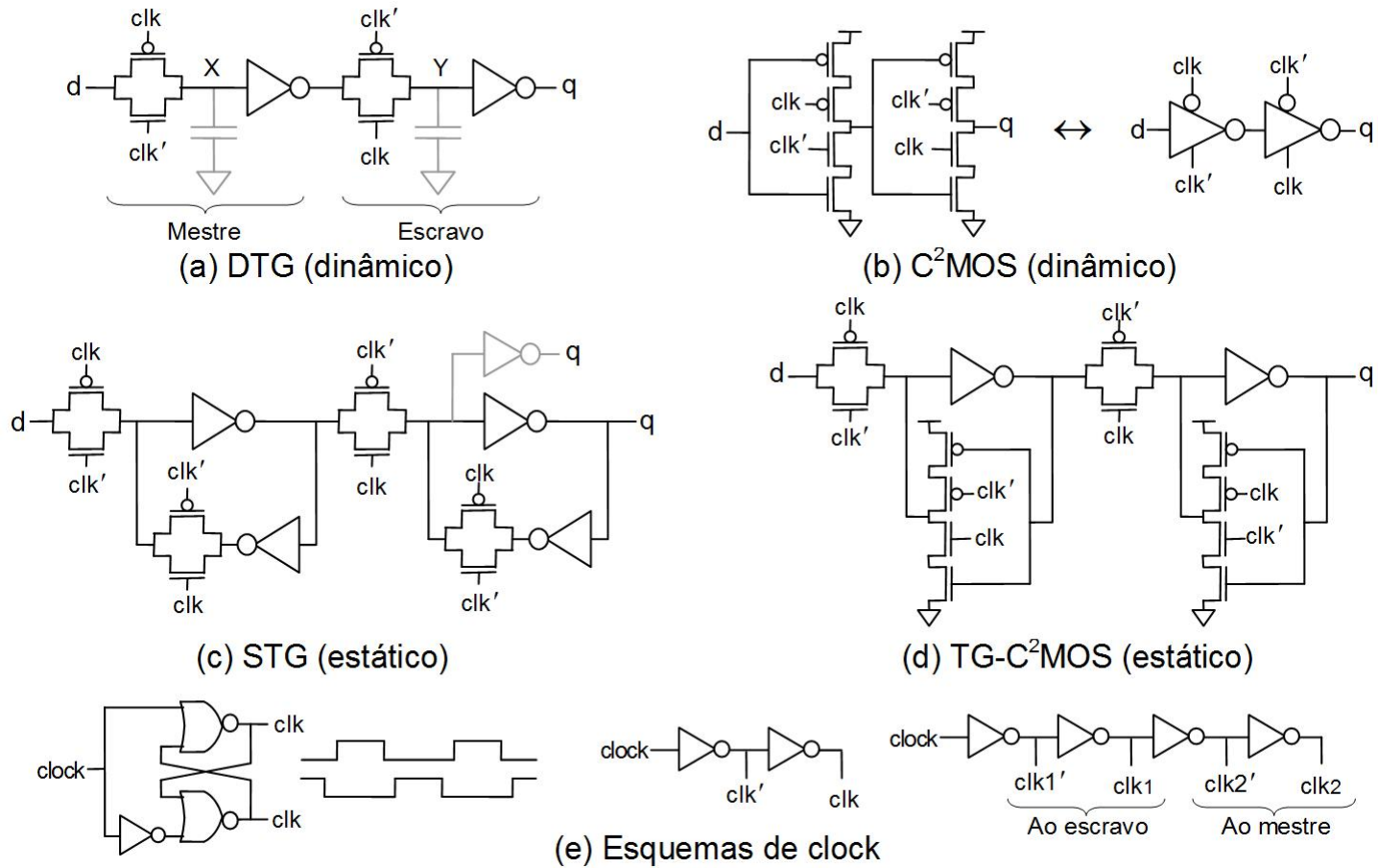


Figura 13.16

Figuras do Capítulo 13

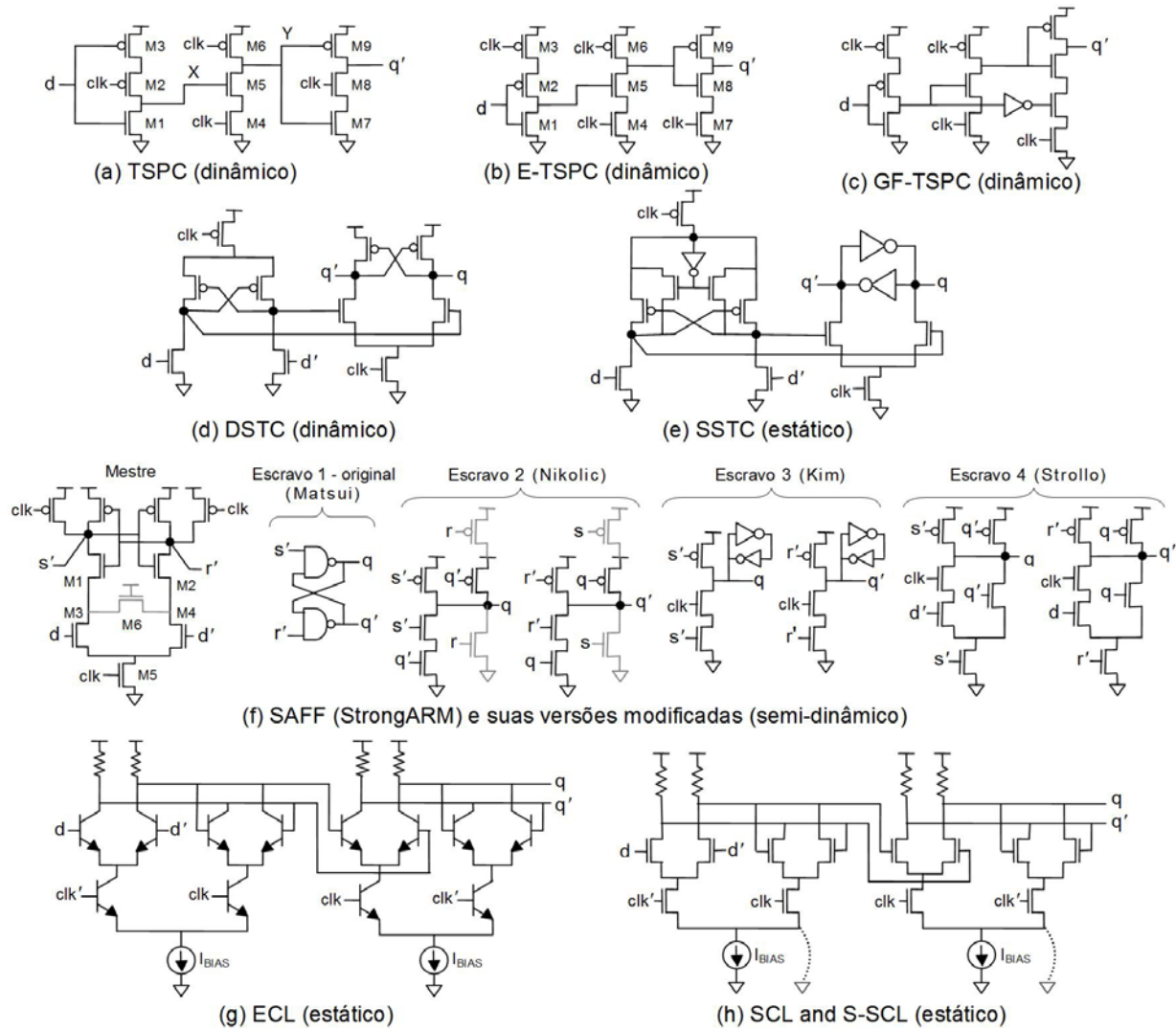


Figura 13.17

Figuras do Capítulo 13

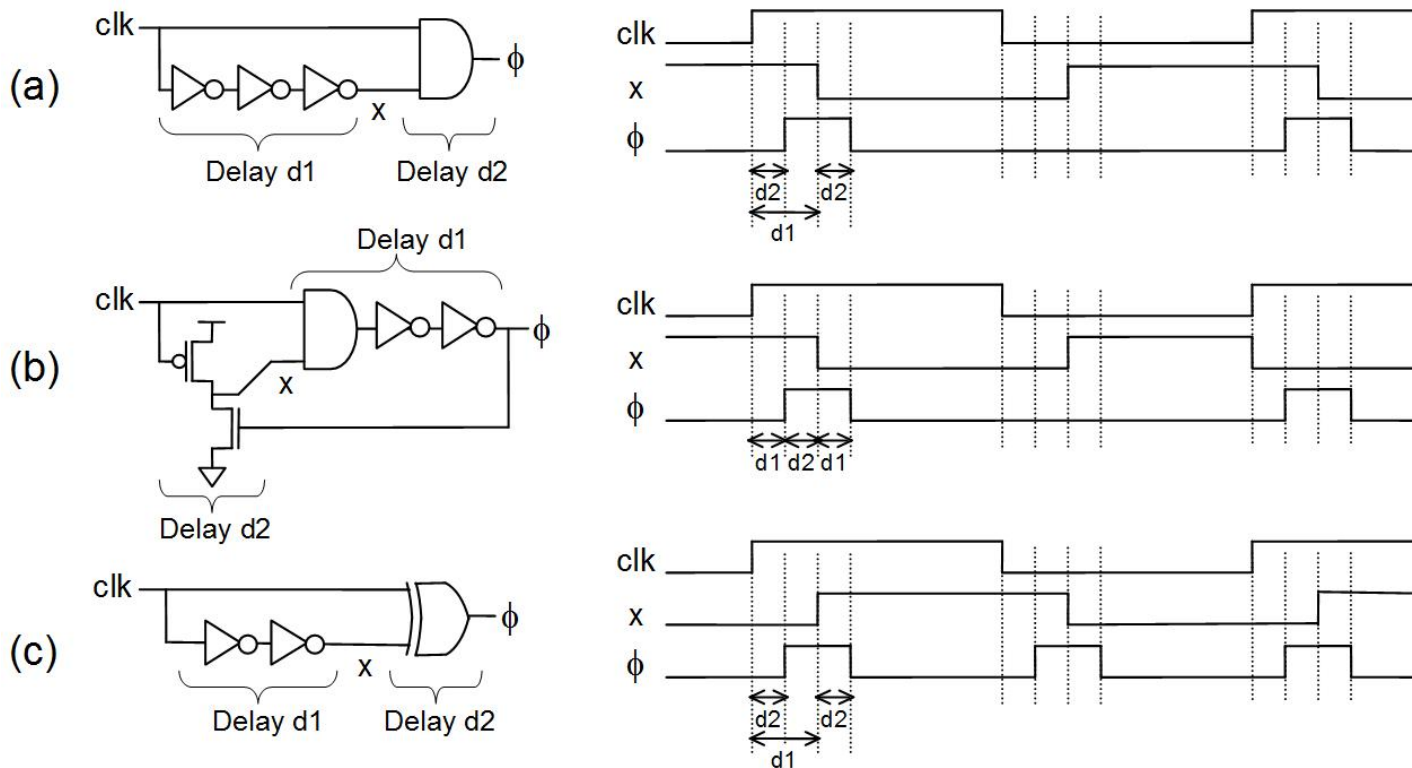


Figura 13.18

Figuras do Capítulo 13

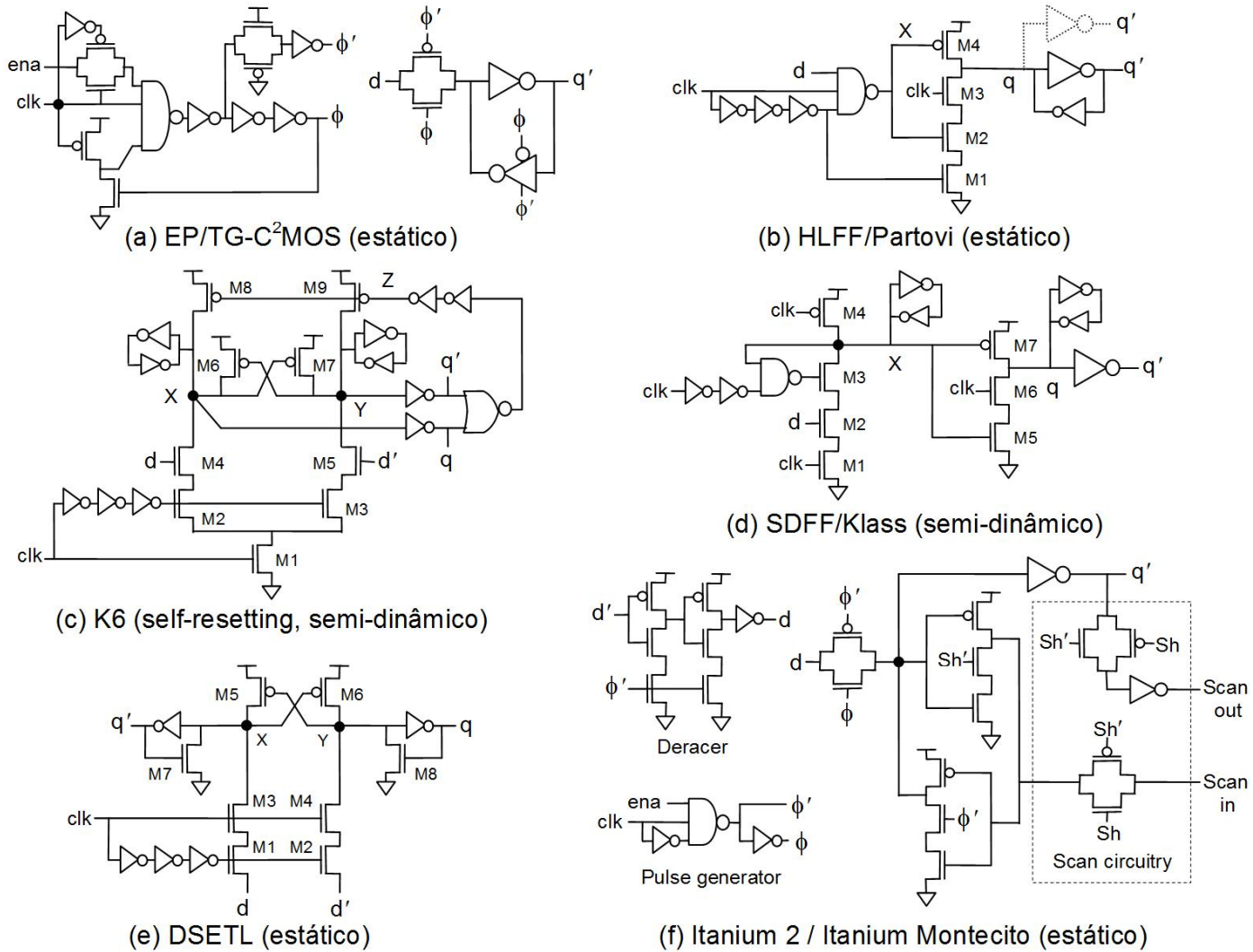
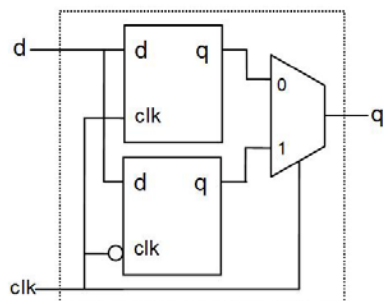
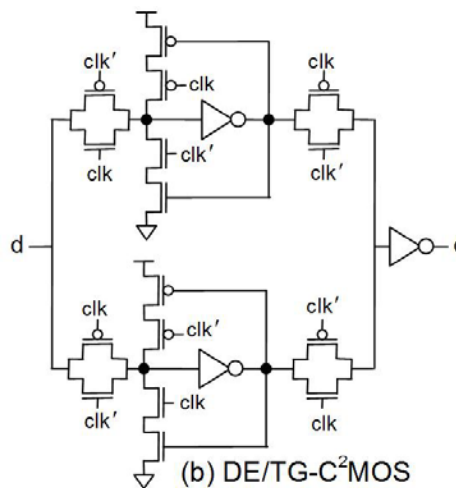


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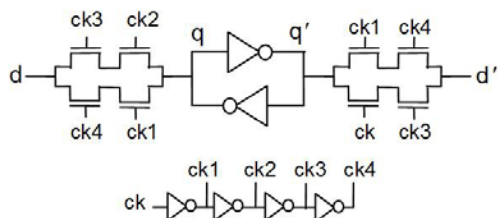
Figuras do Capítulo 13



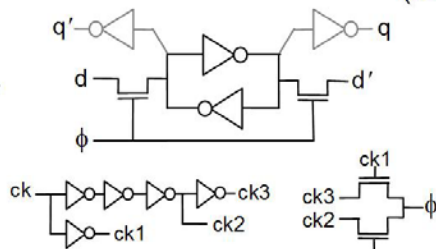
(a) Mux-based dual-edge DFF



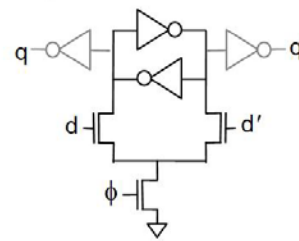
(b) DE/TG-C²MOS (estático)



(c) IP-SRAM (estático)



(d) DSPFF (estático)



(e) DESPFF (estático)

Figura 13.20

Figuras do Capítulo 13

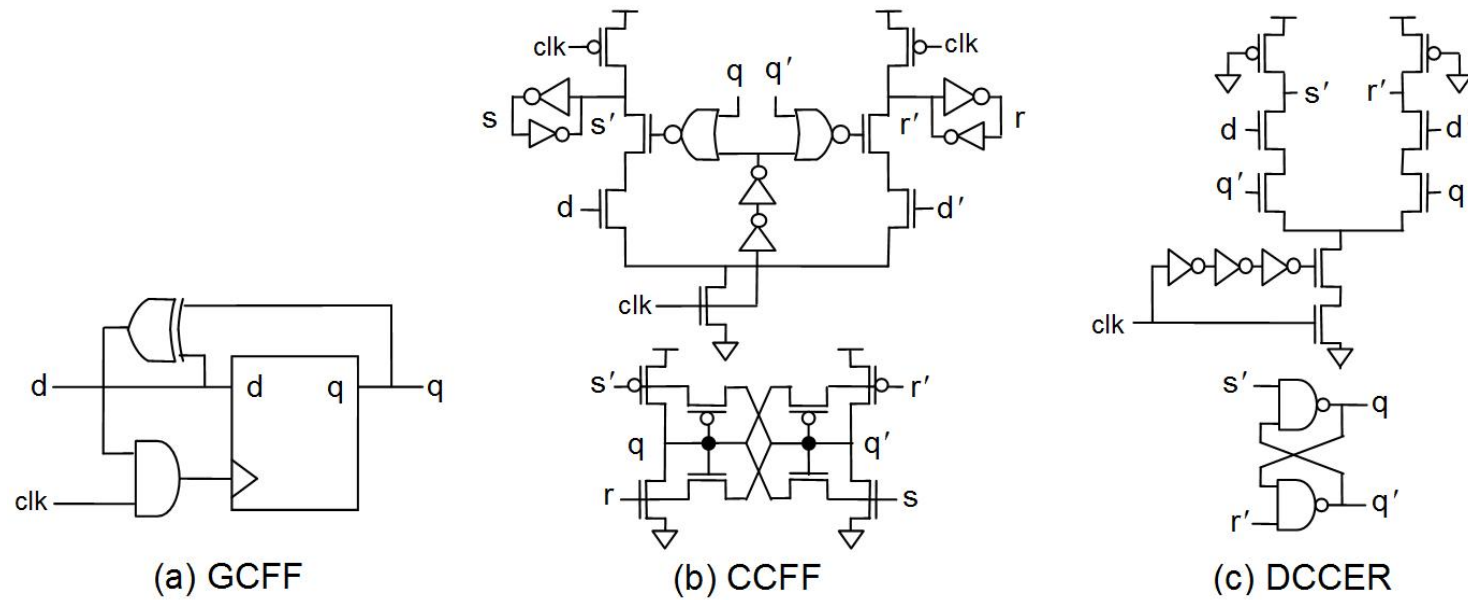


Figura 13.21

Figuras do Capítulo 13

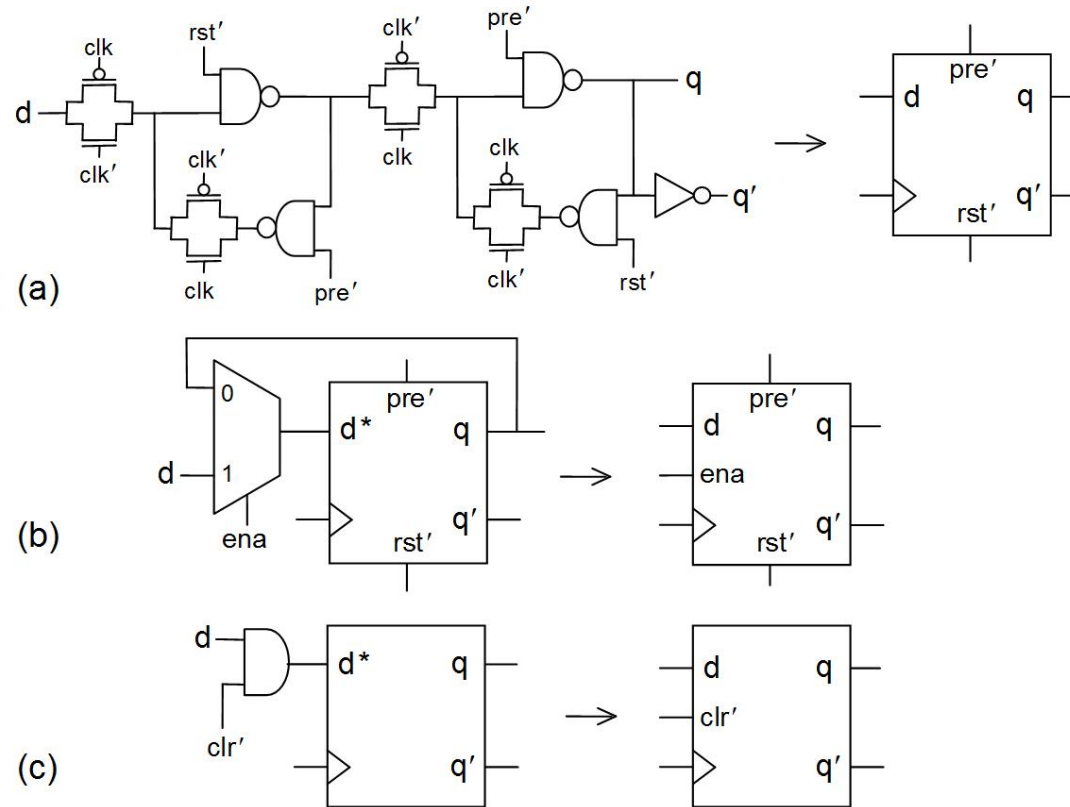


Figura 13.22

Figuras do Capítulo 13

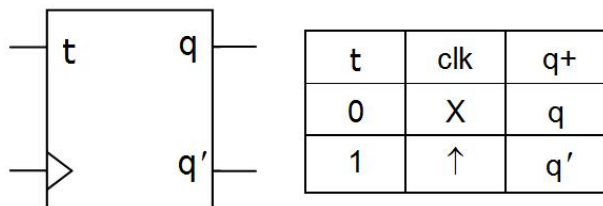
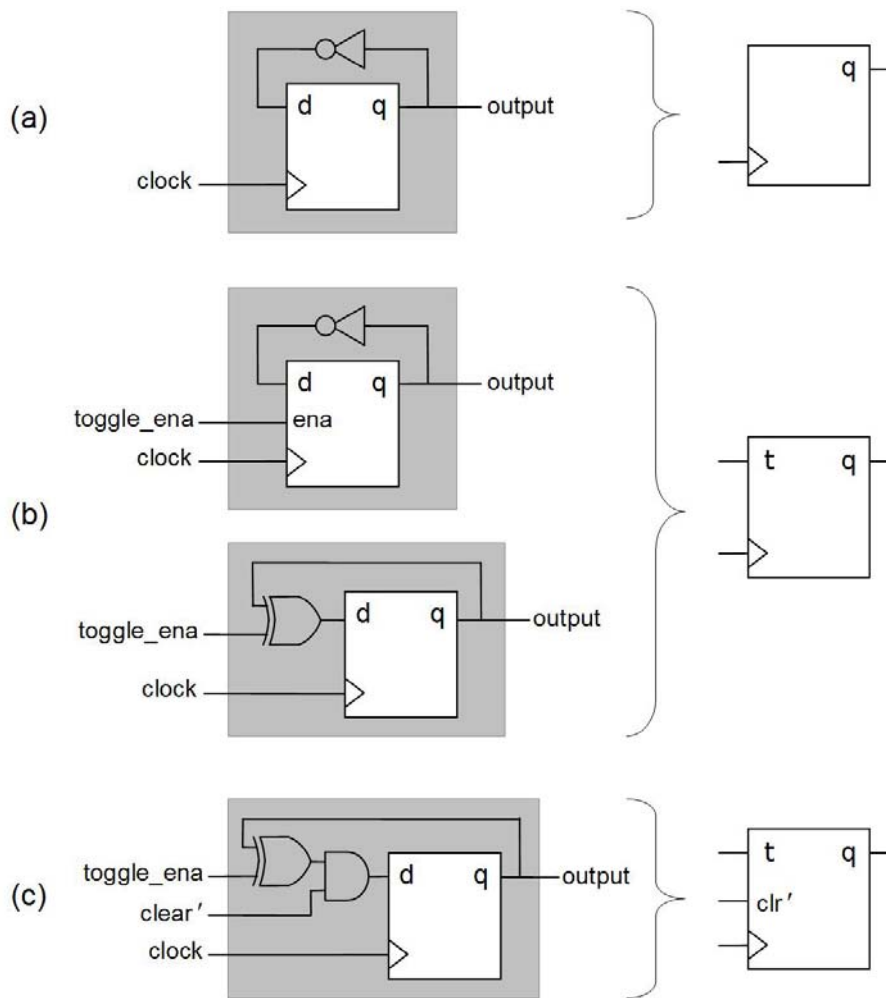


Figura 13.23

Figura 13.24

Figuras do Capítulo 13

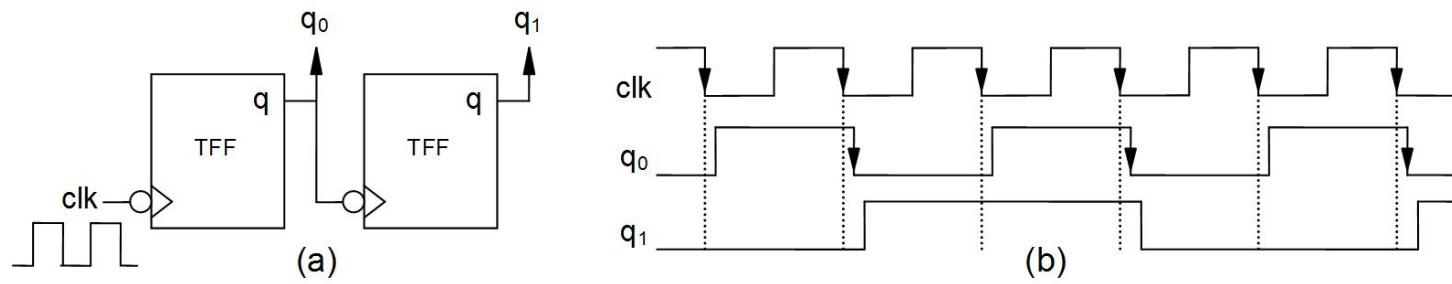


Figura 13.25

Figuras do Capítulo 14

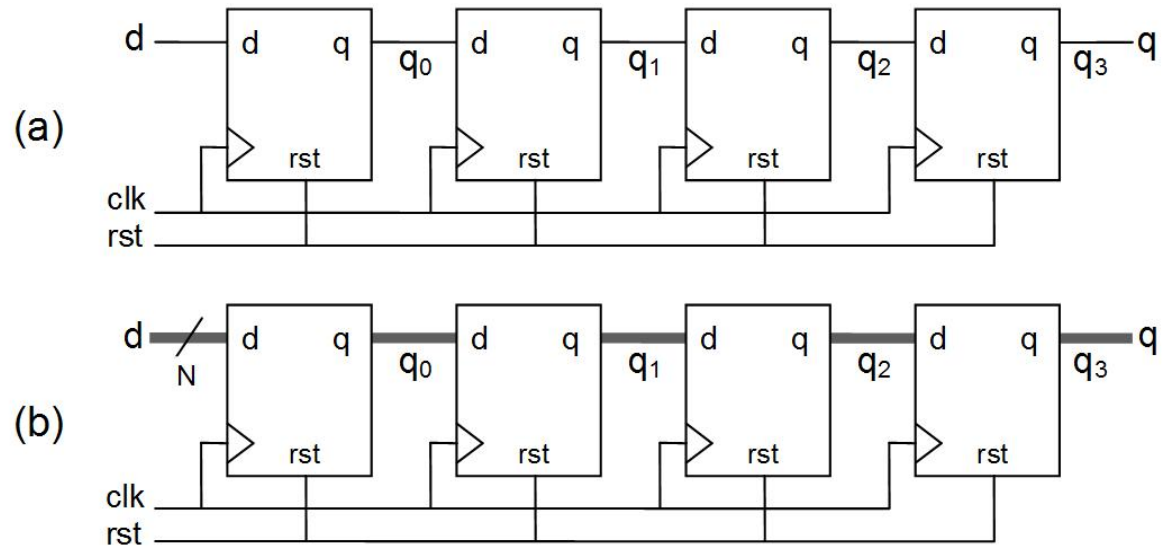


Figura 14.1

Figuras do Capítulo 14

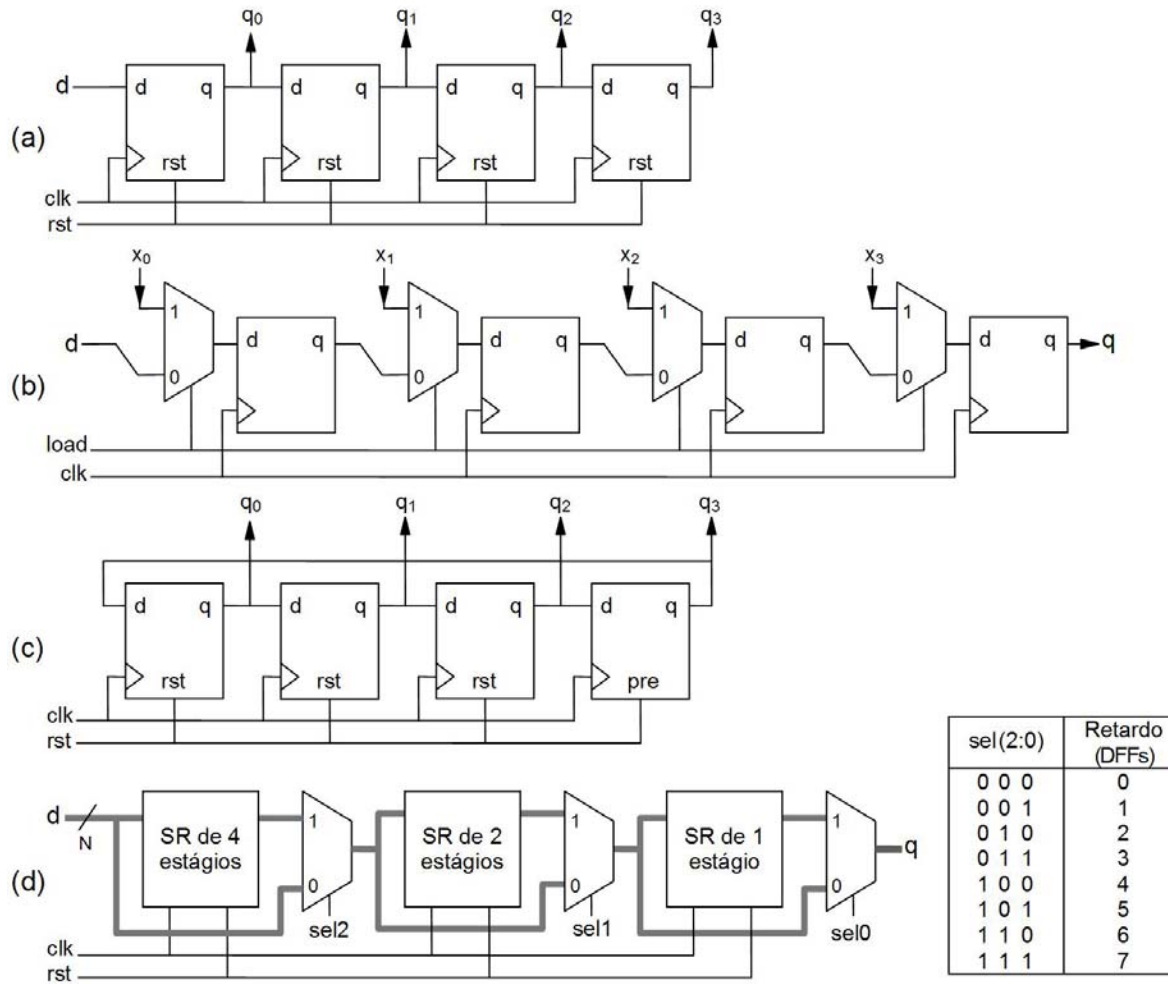


Figura 14.2

Figuras do Capítulo 14

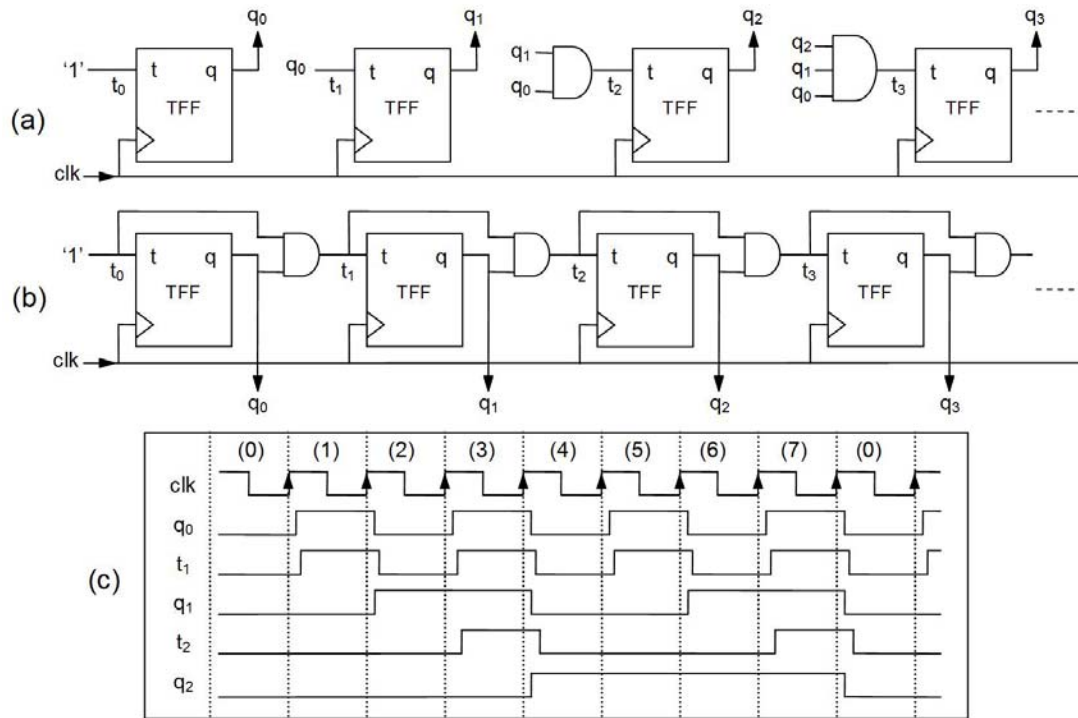


Figura 14.3

q_2 q_1 q_0	Valor decimal	t_2 t_1 t_0
0 0 0	0	0 0 1
0 0 1	1	0 1 1
0 1 0	2	0 0 1
0 1 1	3	1 1 1
1 0 0	4	0 0 1
1 0 1	5	0 1 1
1 1 0	6	0 0 1
1 1 1	7	1 1 1
0 0 0	0	0 0 1
0 0 1	1	0 1 1

Figura 14.4

Figuras do Capítulo 14

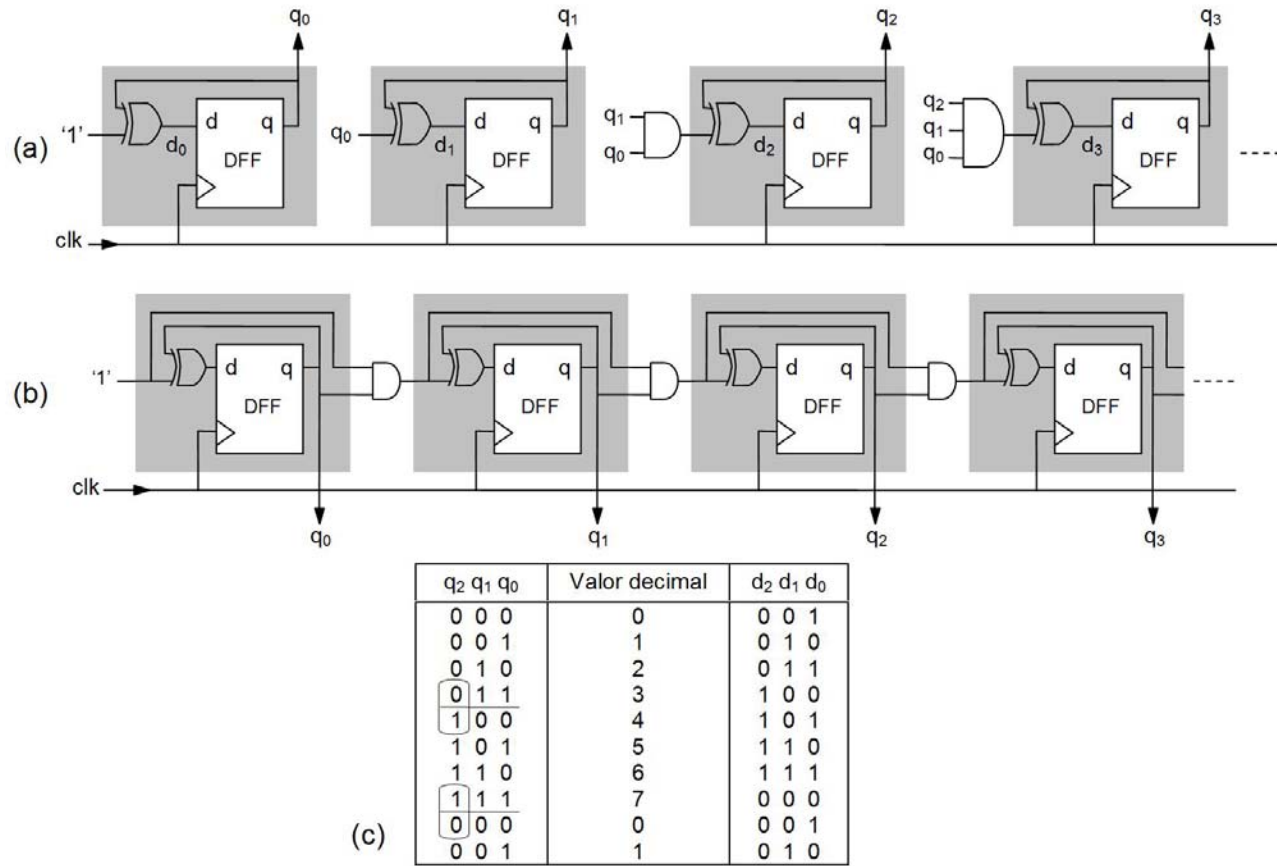


Figura 14.5

Figuras do Capítulo 14

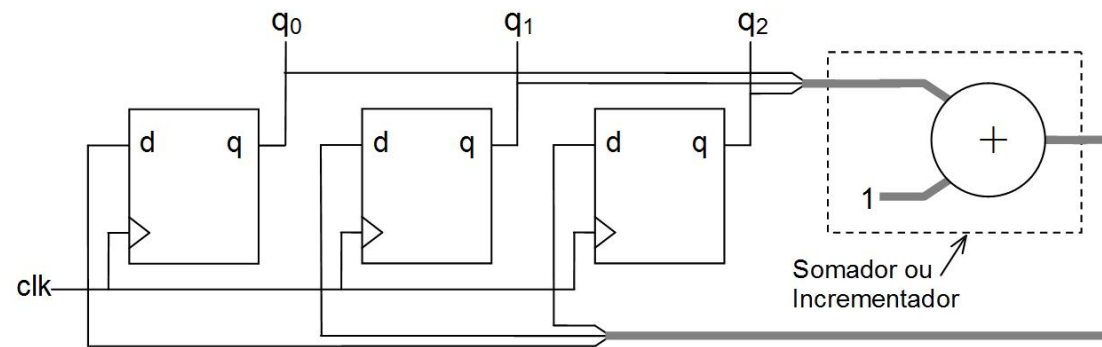


Figura 14.6

Figuras do Capítulo 14

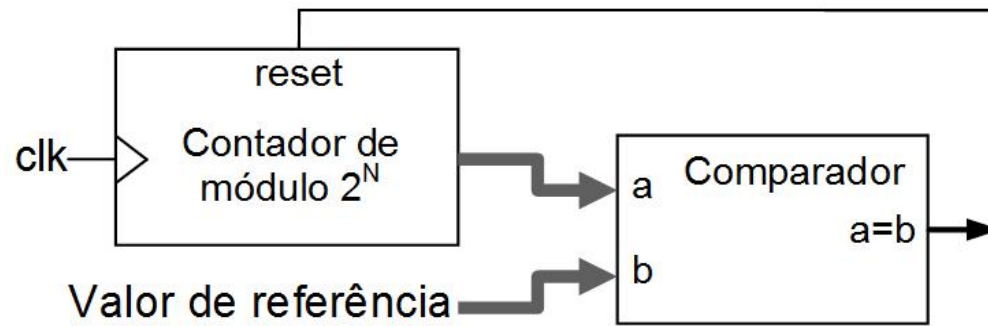


Figura 14.7

Figuras do Capítulo 14

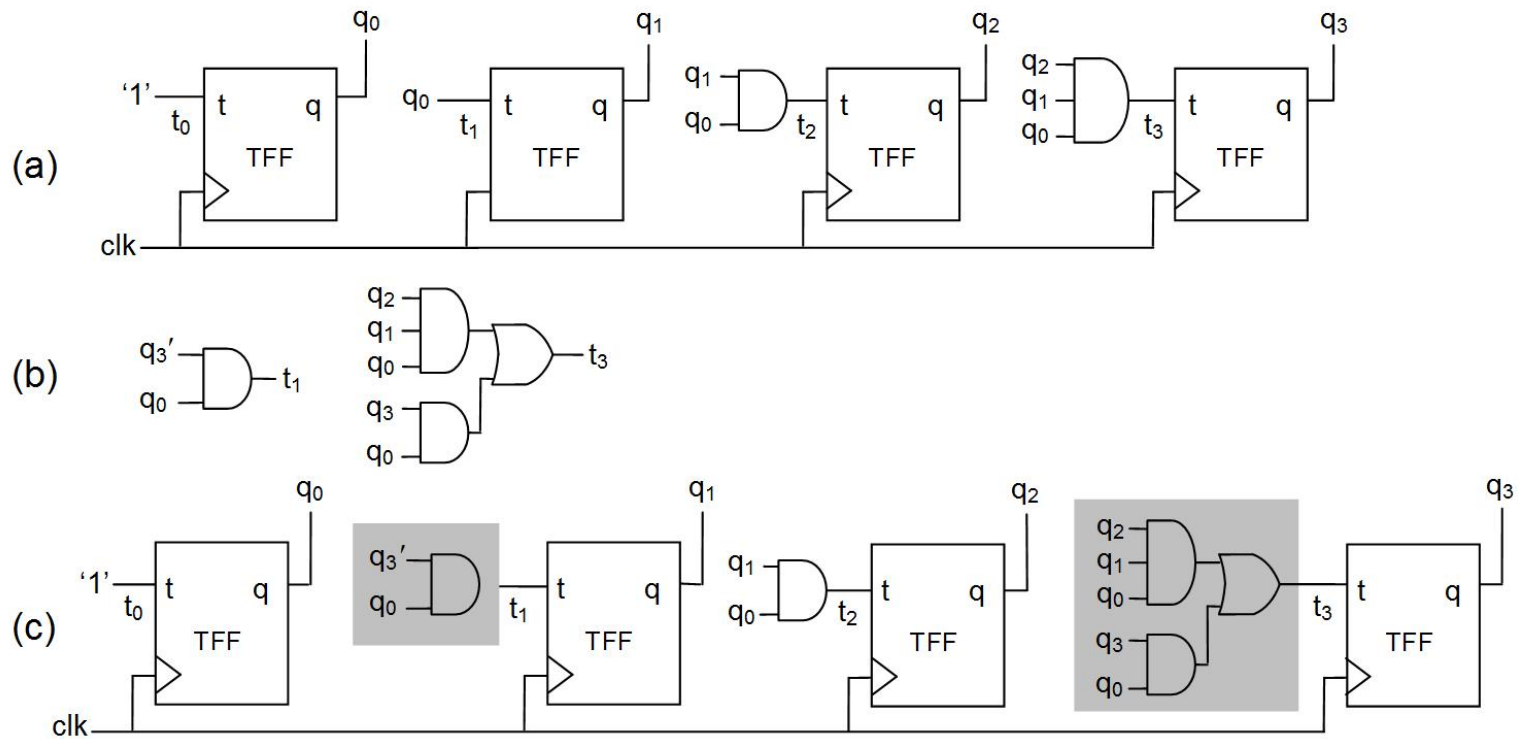


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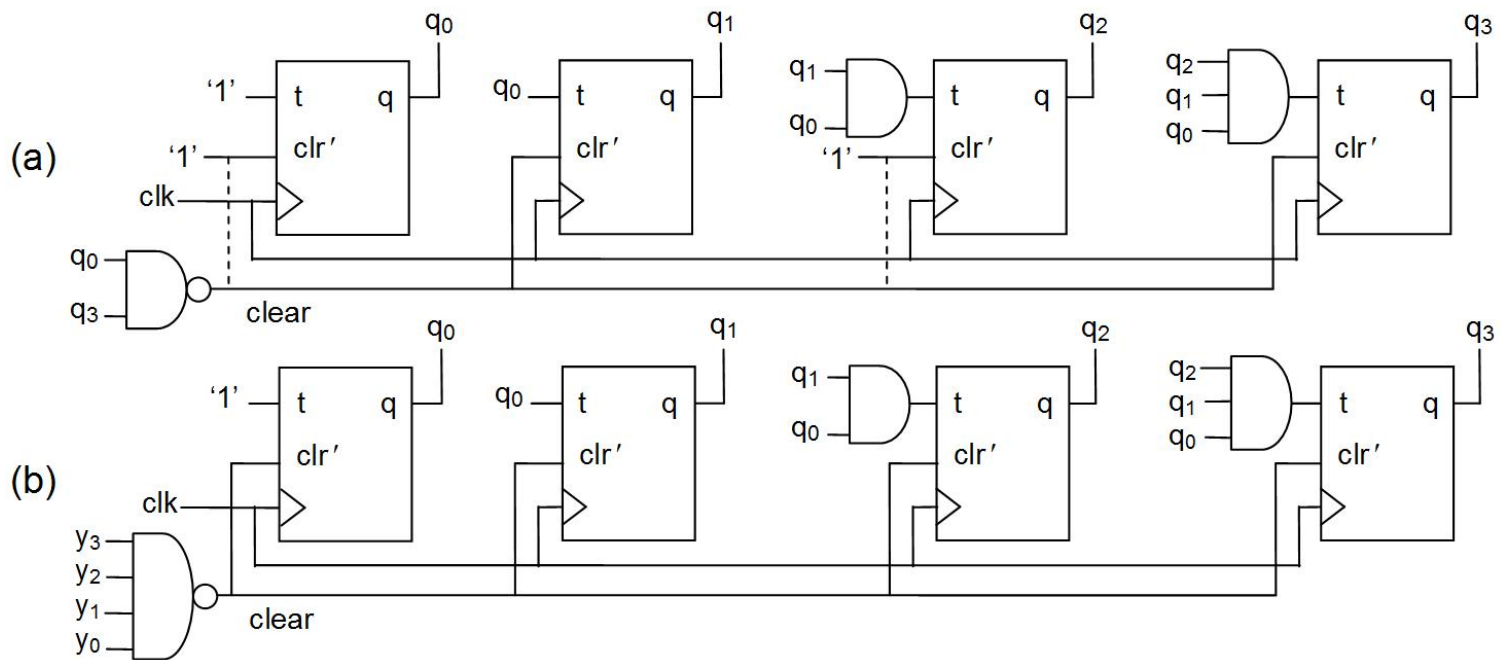


Figura 14.9

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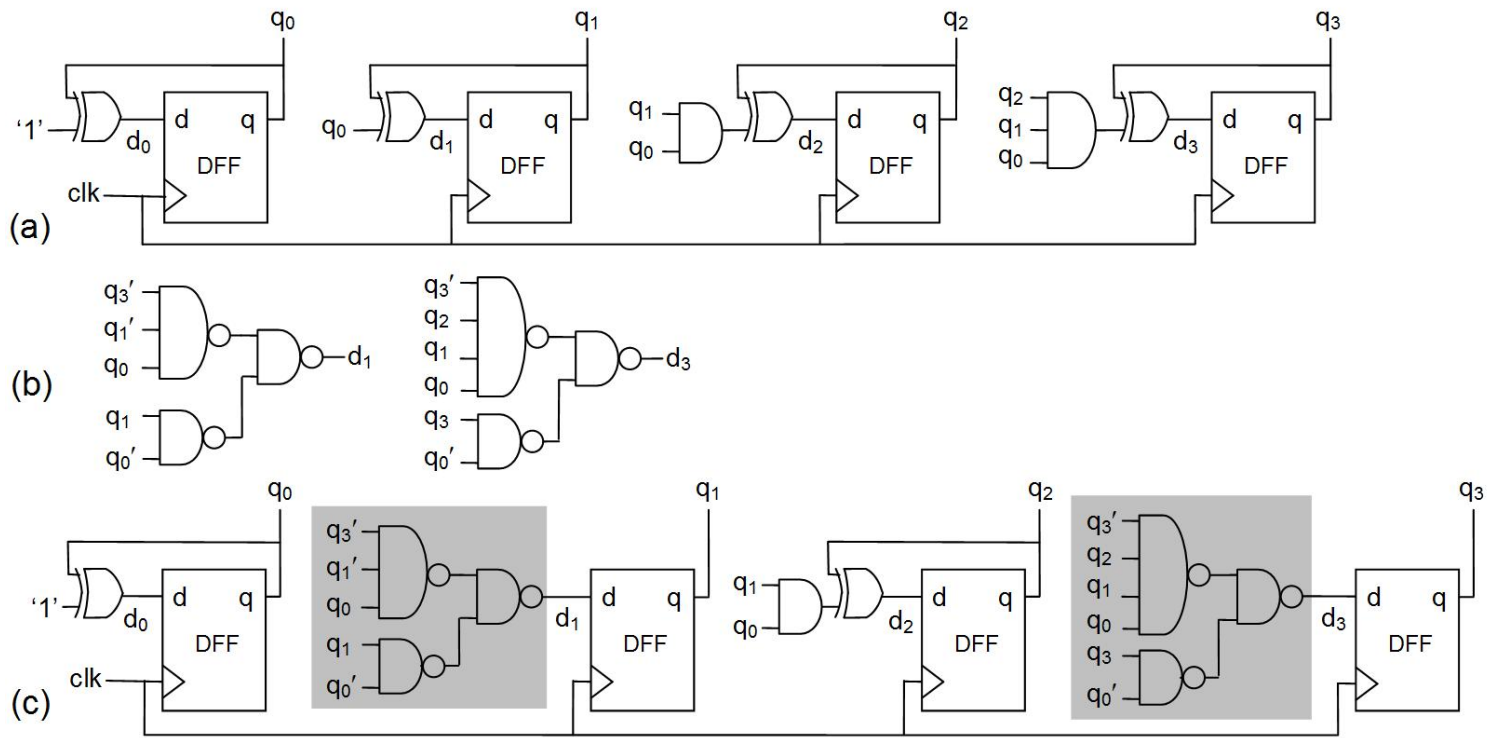


Figura 14.10

Figuras do Capítulo 14

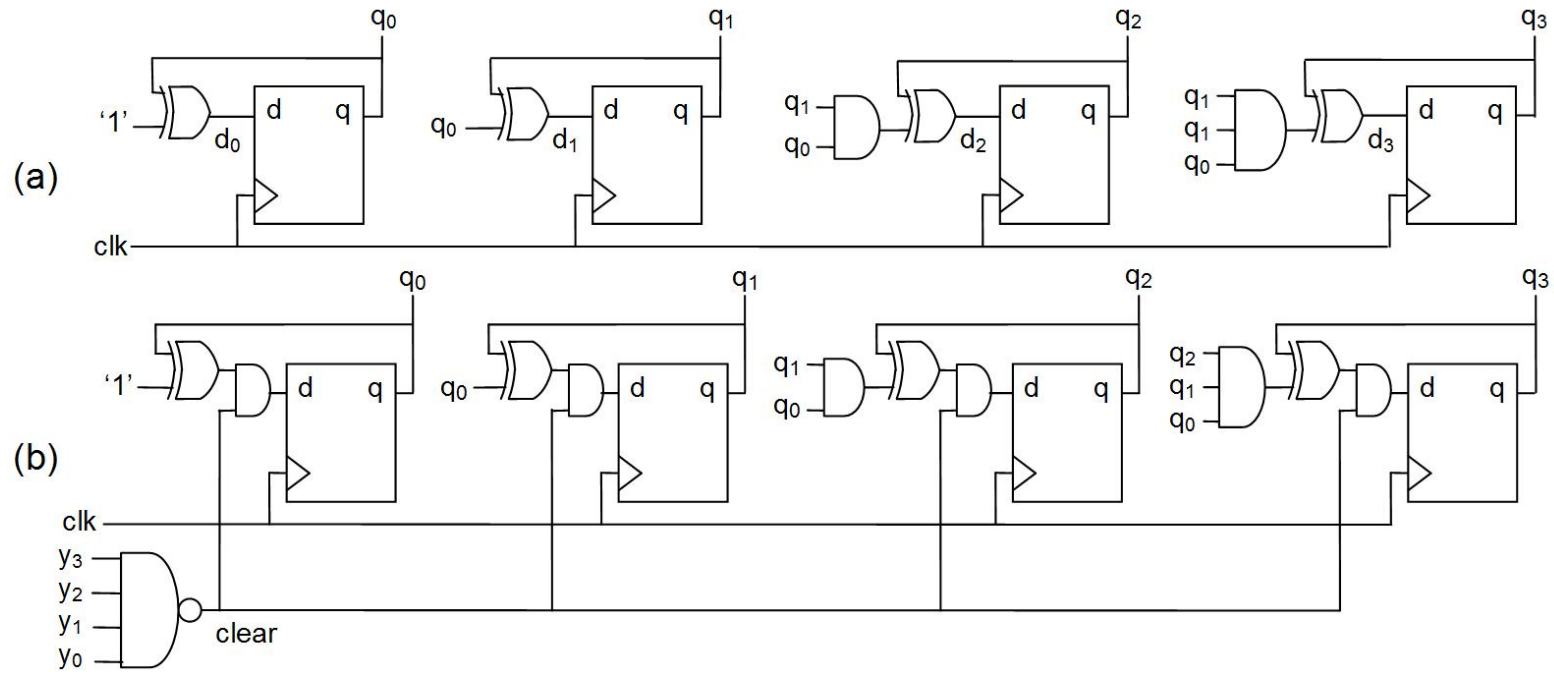


Figura 14.11

Figuras do Capítulo 14

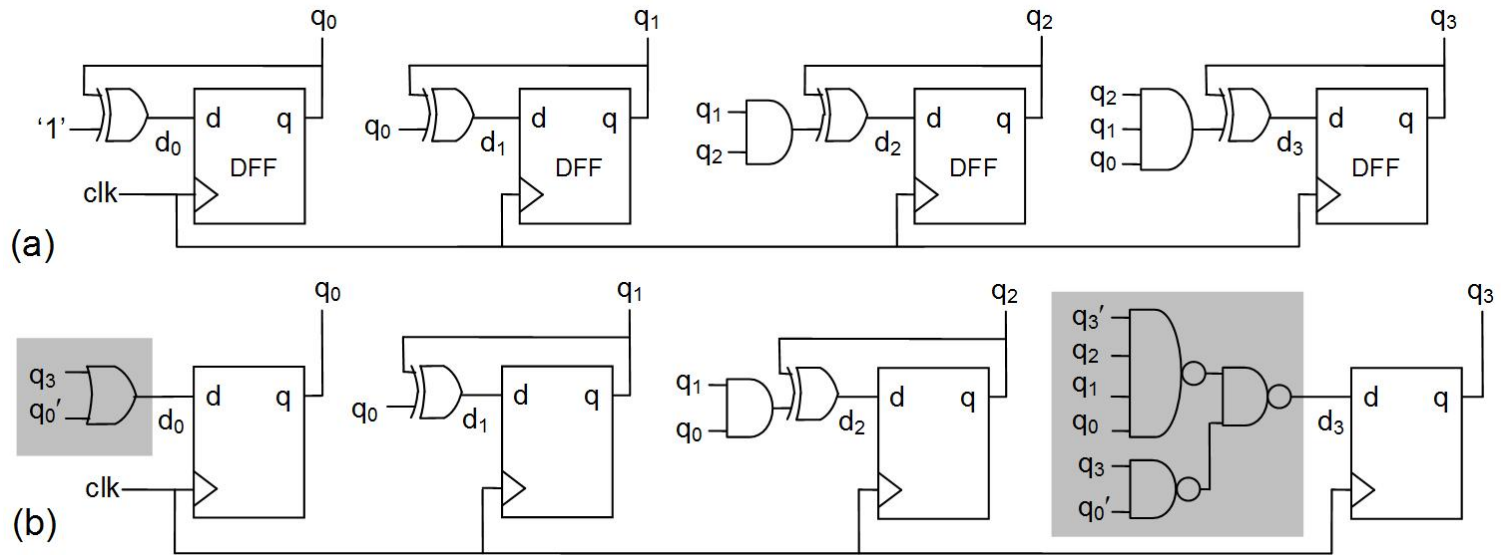


Figura 14.12

Figuras do Capítulo 14

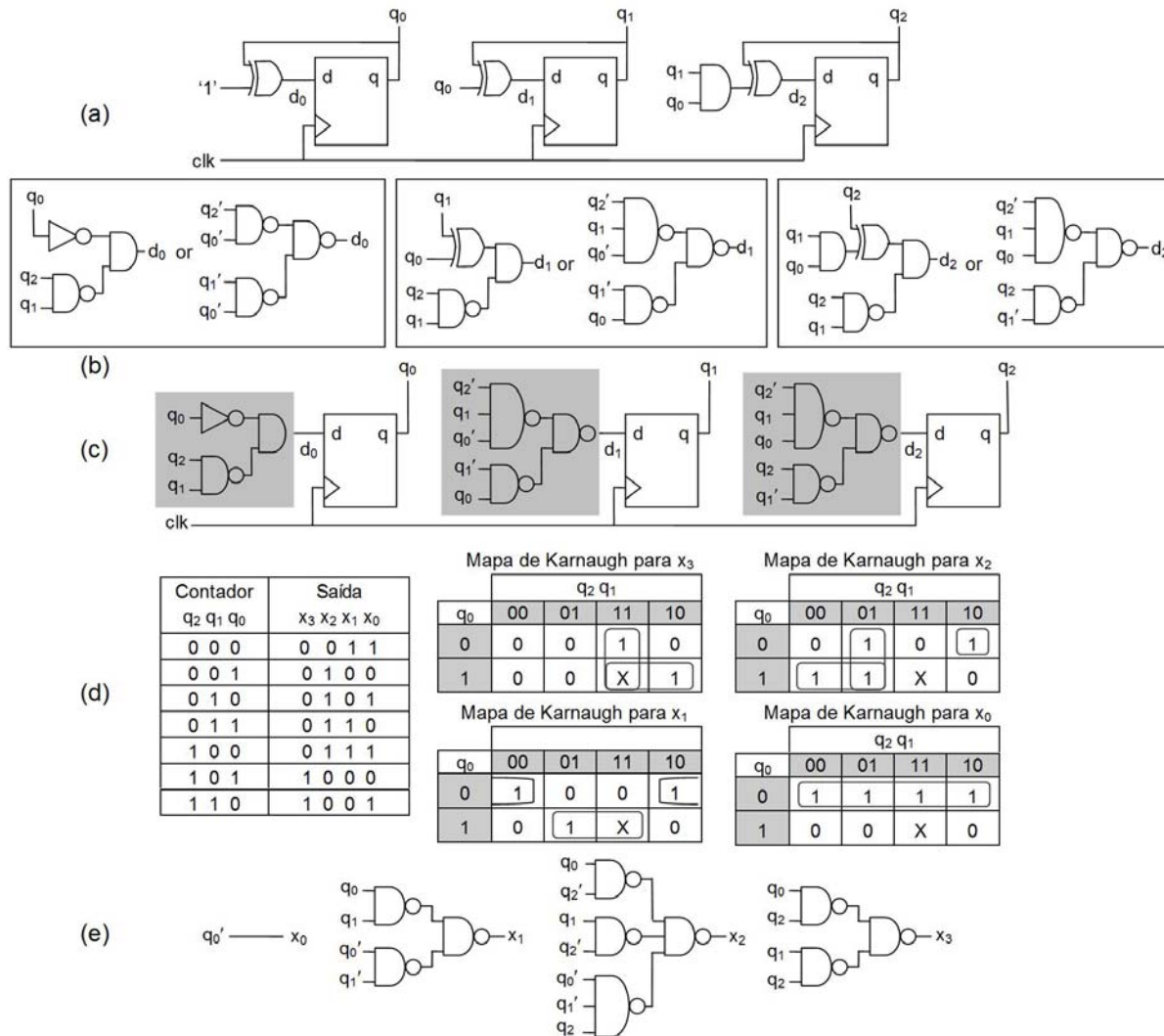


Figura 14.13

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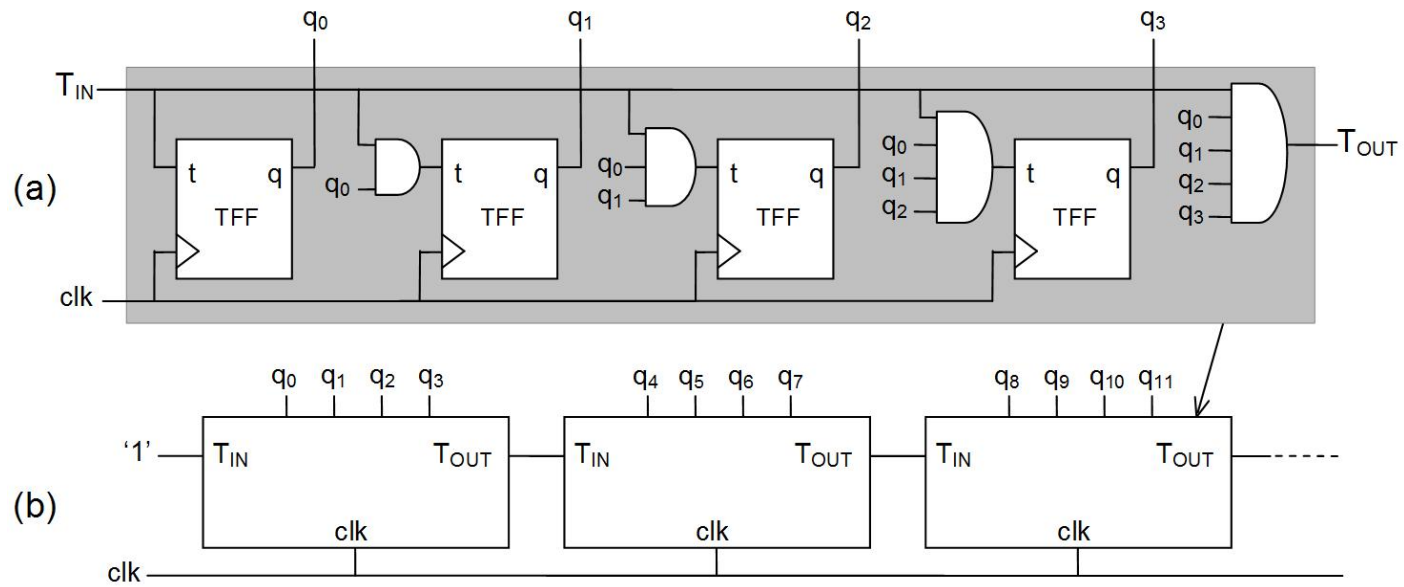


Figura 14.14

Figuras do Capítulo 14

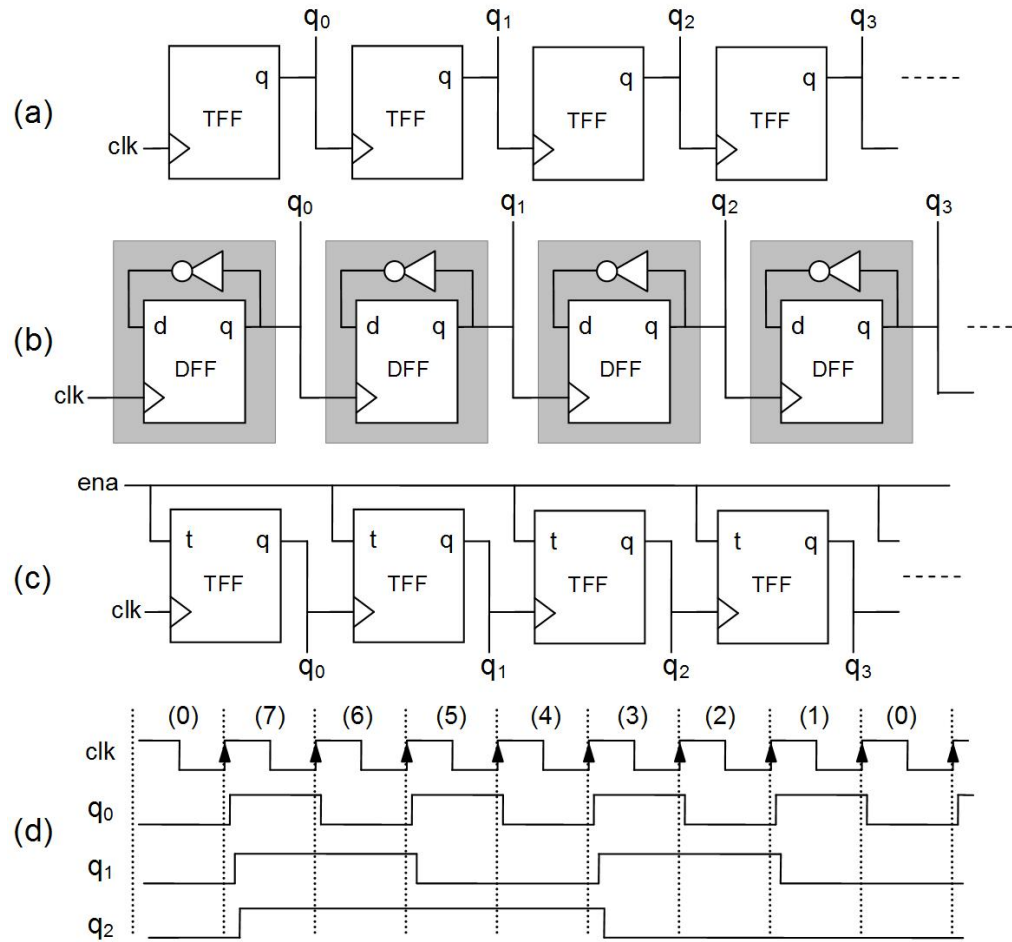


Figura 14.15

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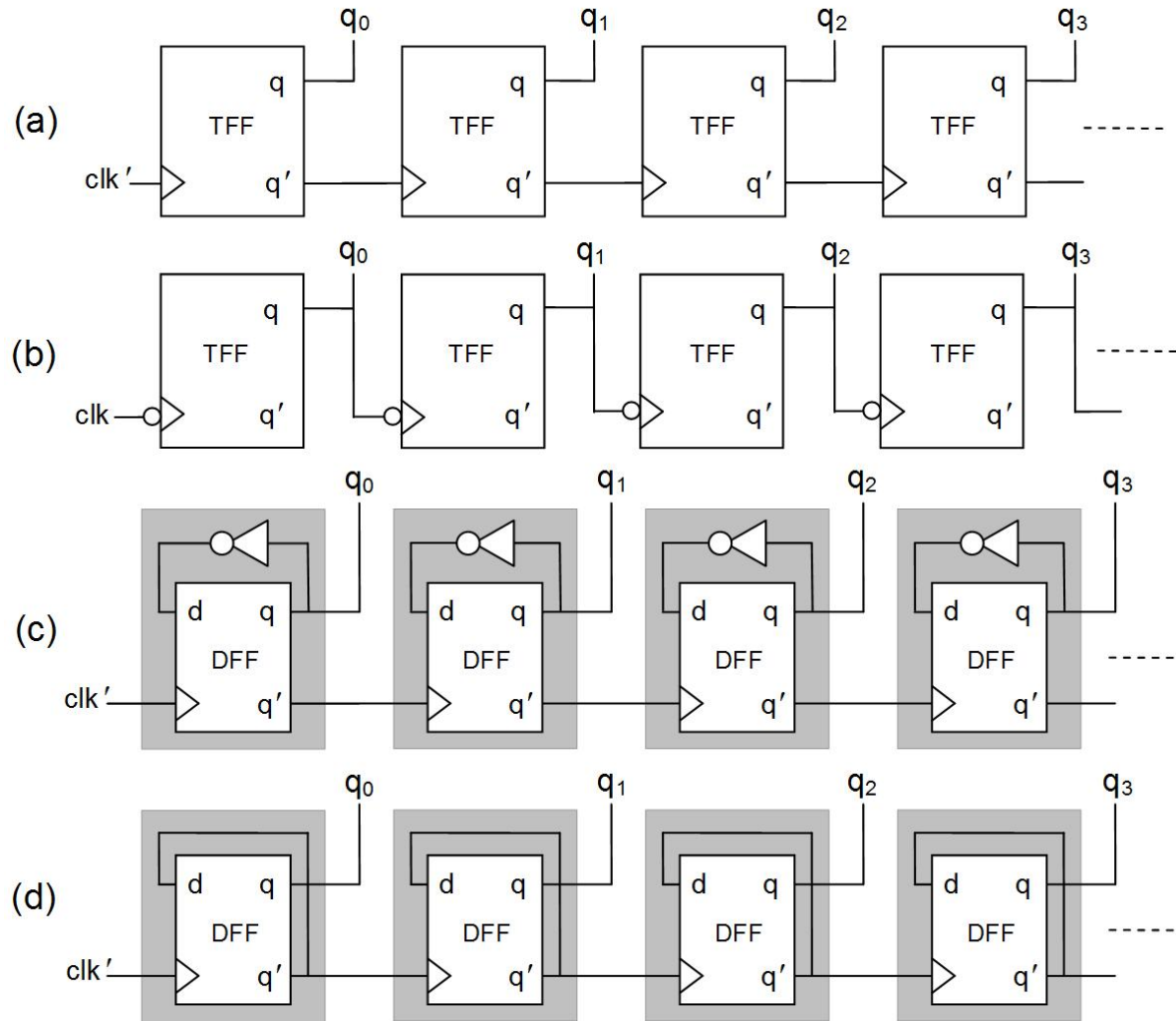


Figura 14.16

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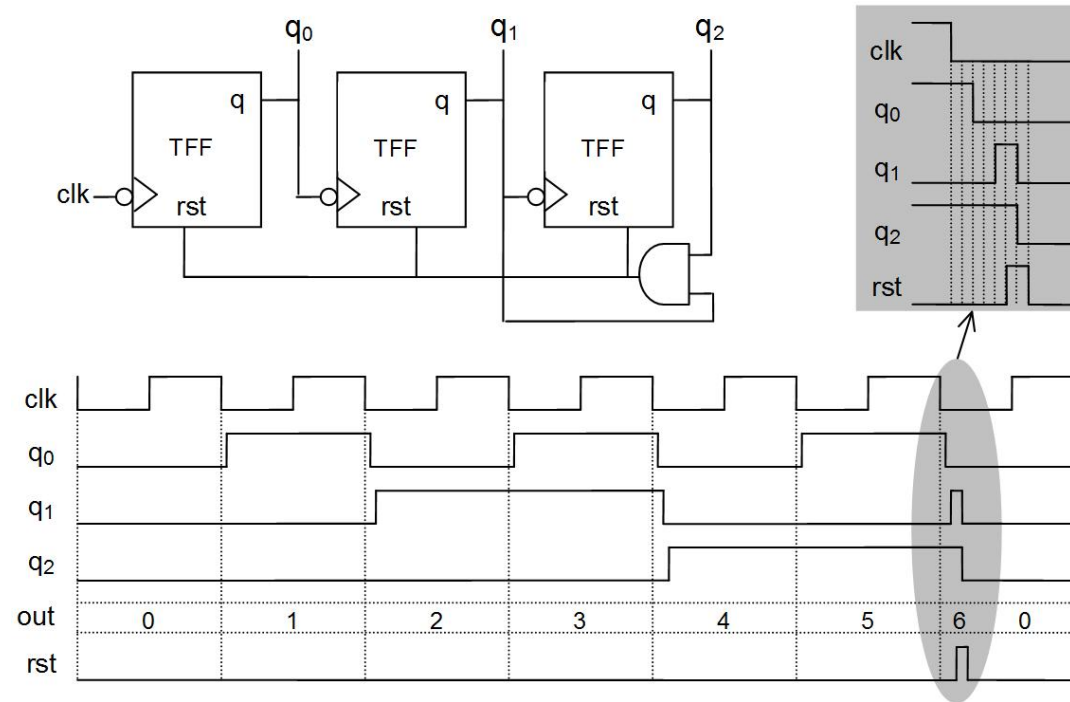


Figura 14.17

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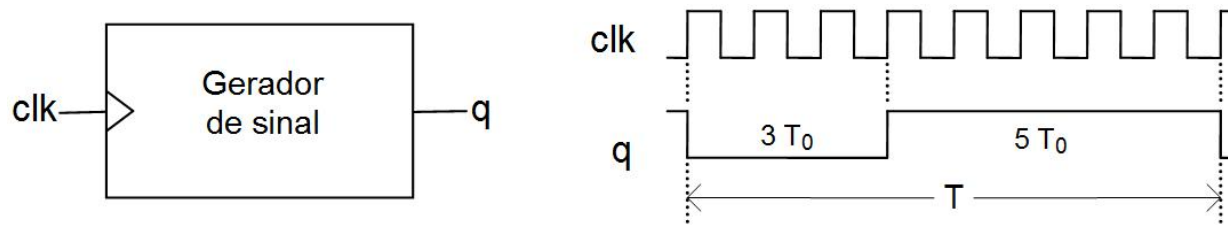


Figura 14.18

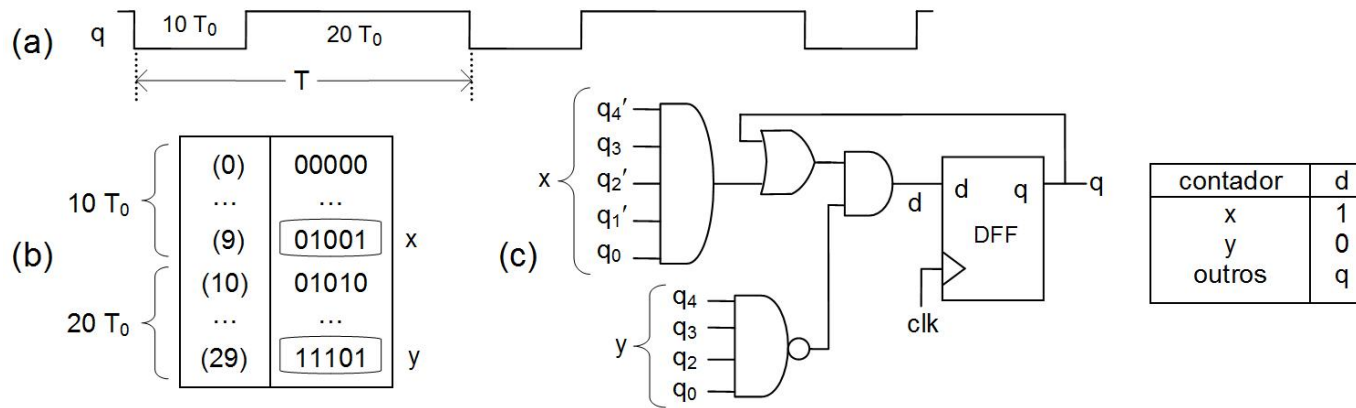


Figura 14.19

Figuras do Capítulo 14

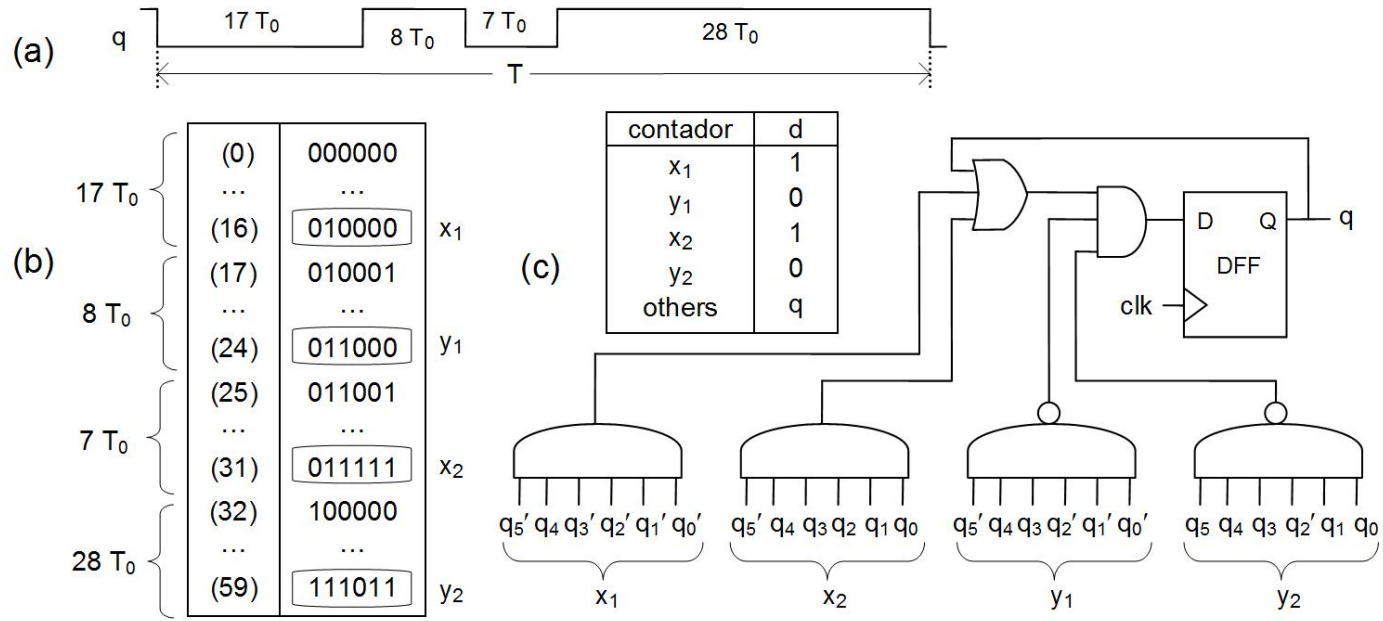


Figura 14.20

Figuras do Capítulo 14

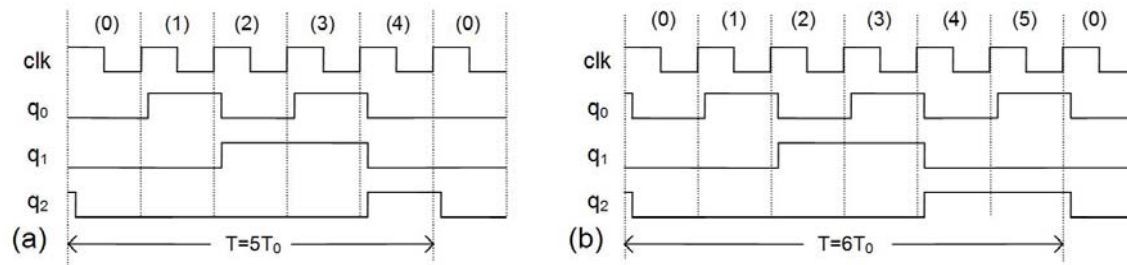


Figura 14.21

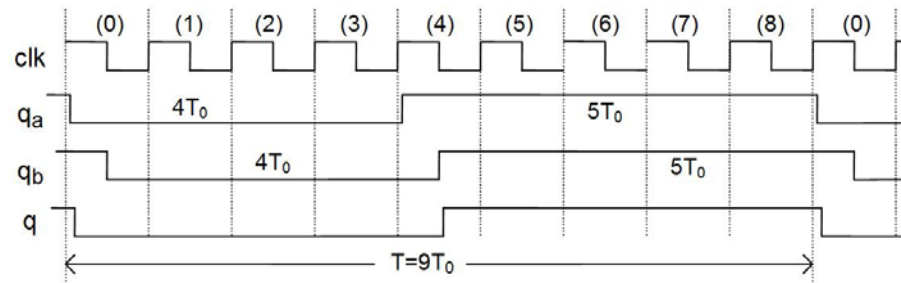


Figura 14.22

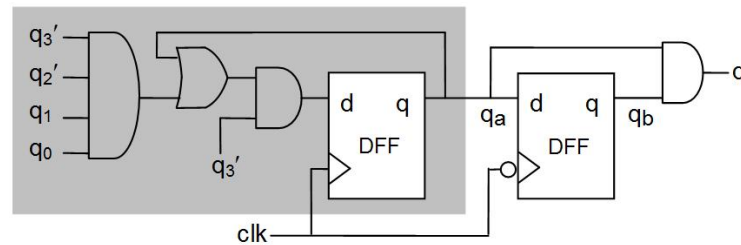


Figura 14.23

Figuras do Capítulo 14

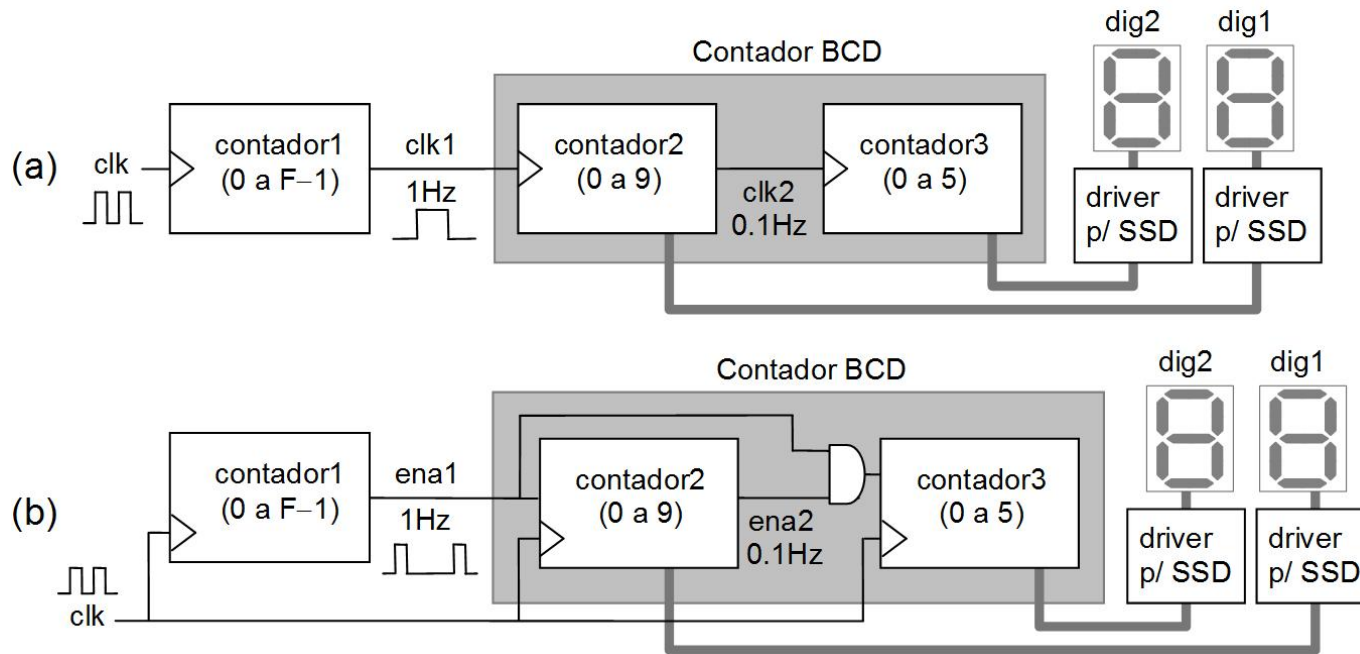


Figura 14.24

Figuras do Capítulo 14

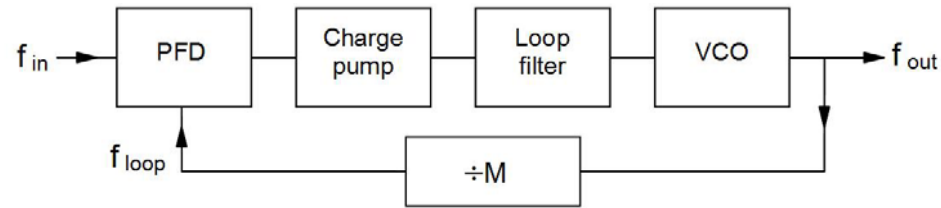


Figura 14.25

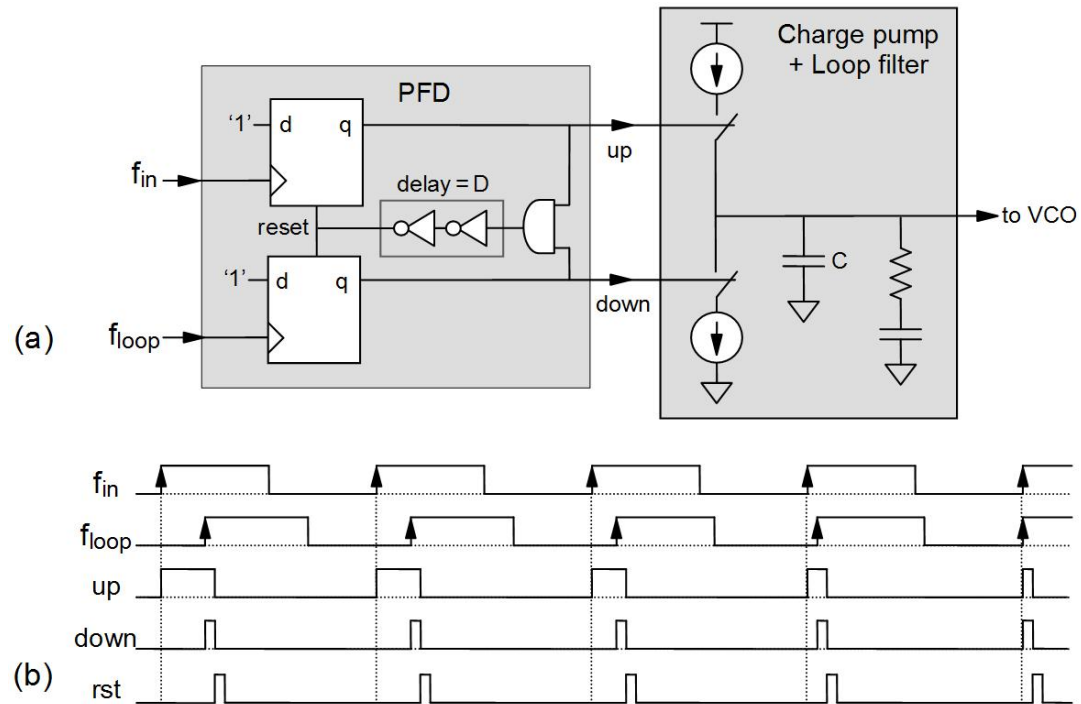


Figura 14.26

Figuras do Capítulo 14

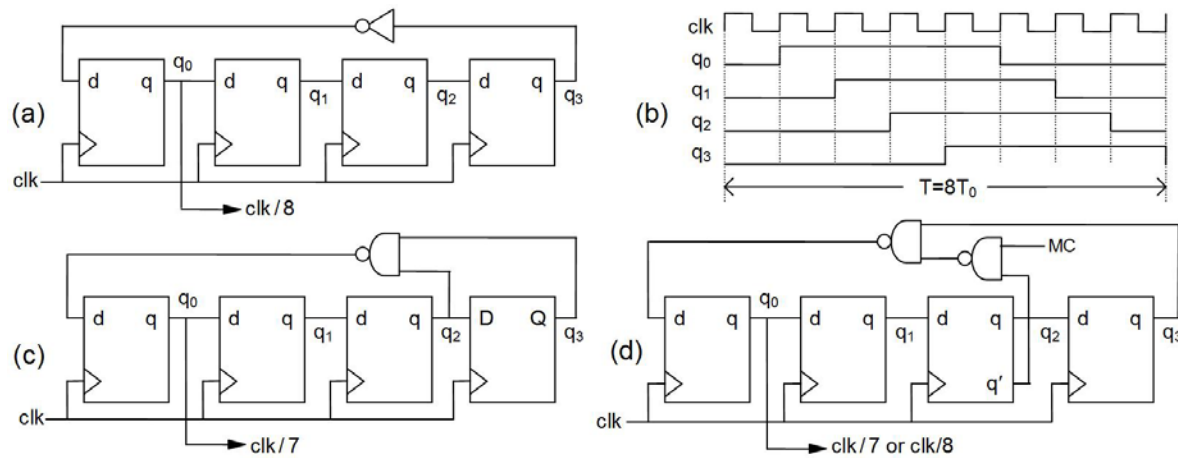


Figura 14.27

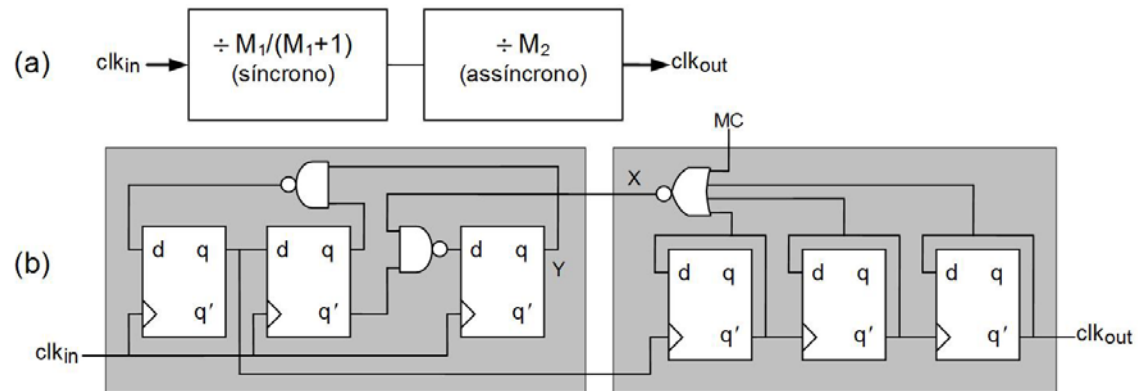


Figura 14.28

Figuras do Capítulo 14

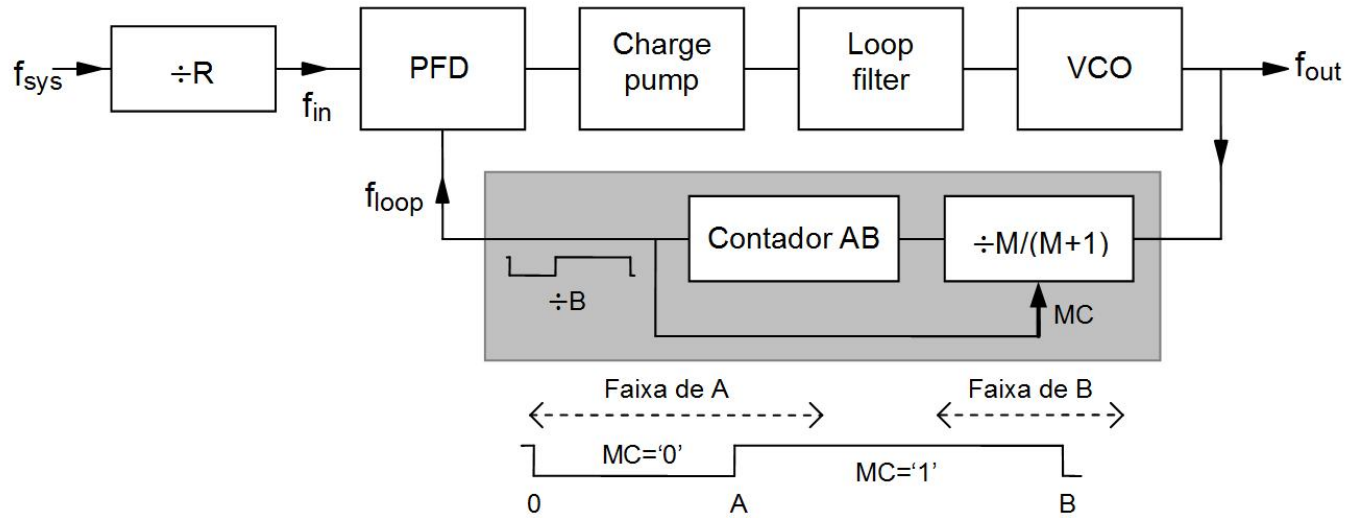


Figura 14.29

Figuras do Capítulo 14

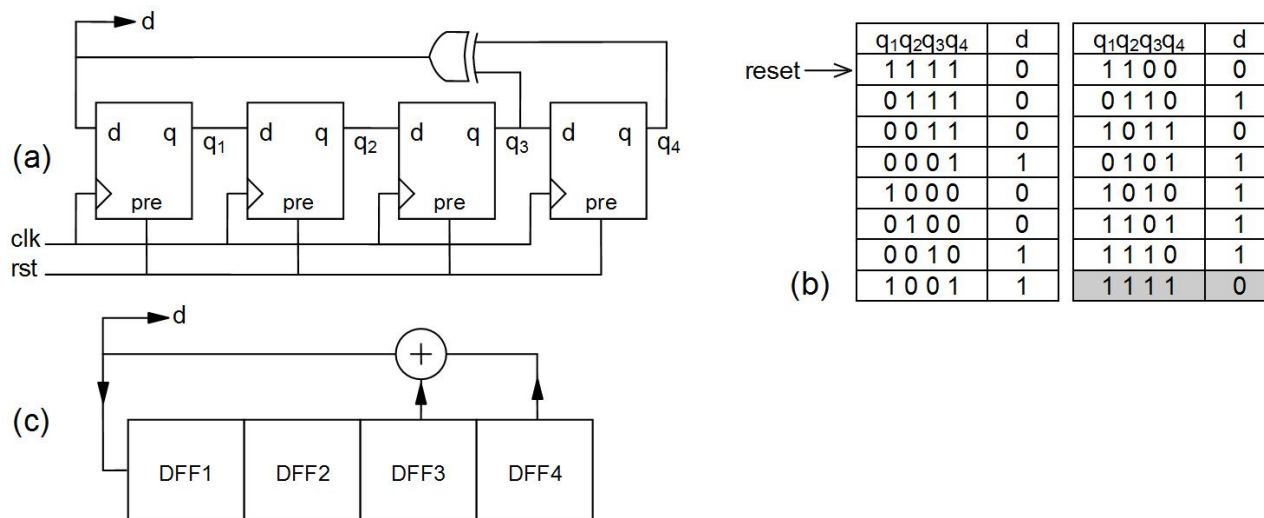


Figura 14.30

N (flip-flops)	Polinômio característico
3	$1 + x^2 + x^3$
4	$1 + x^3 + x^4$
5	$1 + x^3 + x^5$
6	$1 + x^5 + x^6$
7	$1 + x^6 + x^7$
8	$1 + x^1 + x^6 + x^7 + x^8$
9	$1 + x^5 + x^9$
15	$1 + x^{14} + x^{15}$
16	$1 + x^4 + x^{13} + x^{15} + x^{16}$
32	$1 + x^{10} + x^{30} + x^{31} + x^{32}$

Figura 14.31

Figuras do Capítulo 14

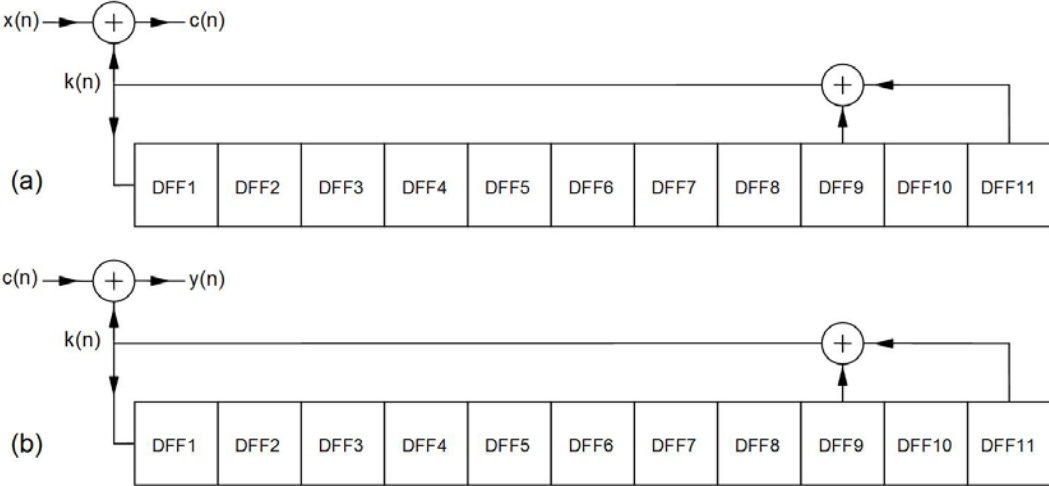


Figura 14.32

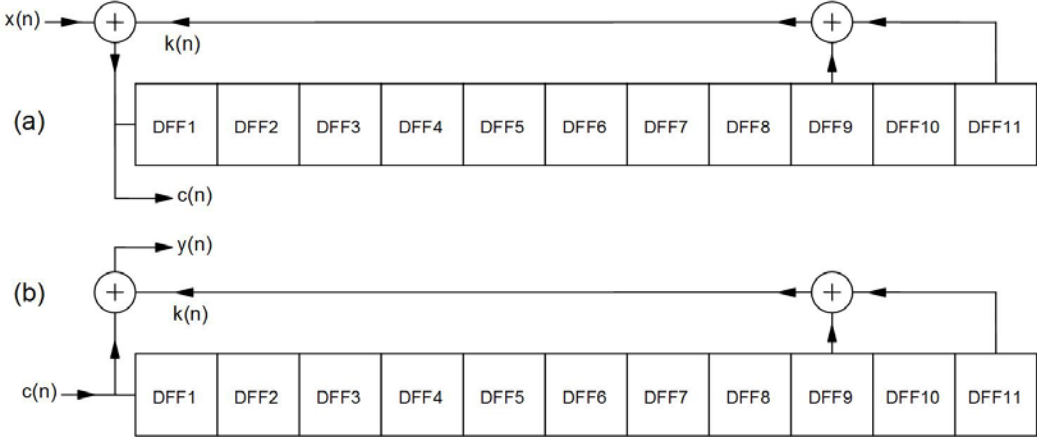


Figura 14.33

Figuras do Capítulo 14

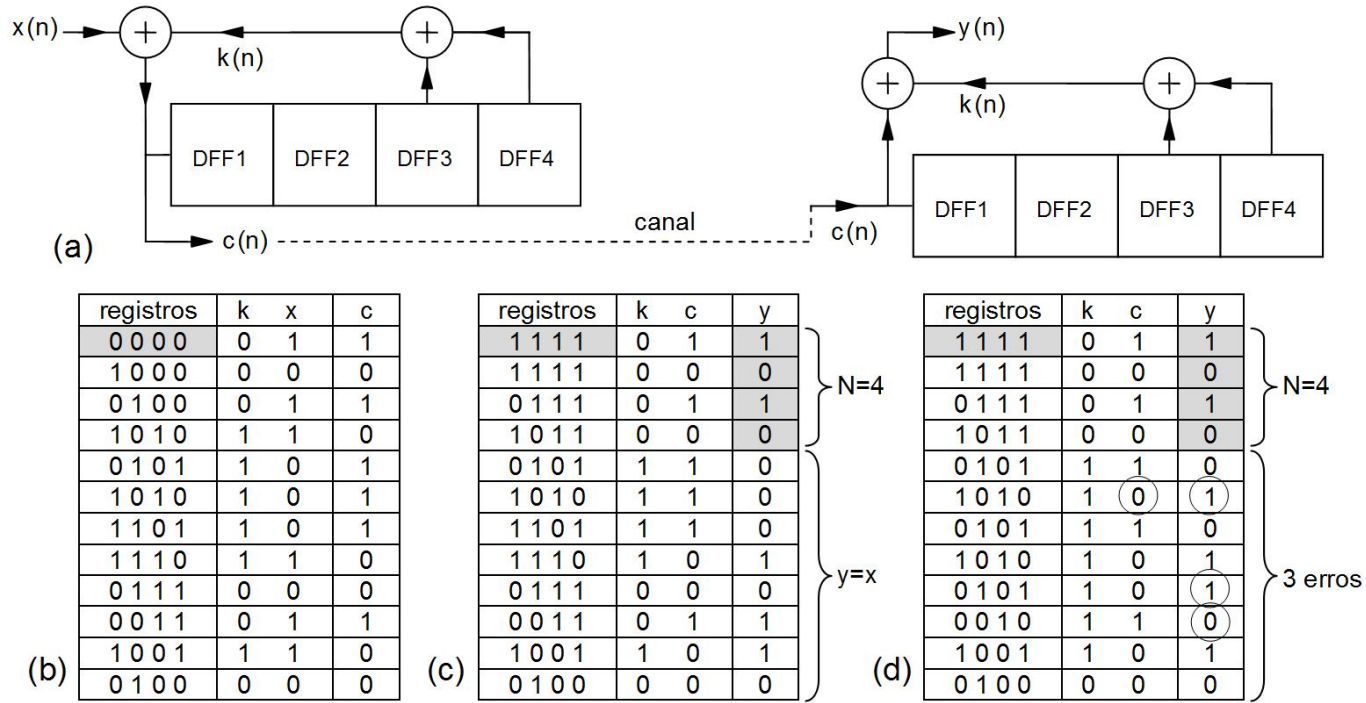


Figura 14.34